Abstract Silicon (Si) based RF-IC's become the key components to realize low cost single chip RF sections for mobile communication terminals. The latest Si process technologies have offered ultra short gate CMOS FET's and novel SiGe HBT's, therefore RF performances of Si based RF-IC's have been rapidly improved and these transistor's performances are approaching to those of GaAs FETs. To realize single chip RF sections, there is a problem of high-loss on-chip passive components due to the dielectric loss of Si substrates. High resistivity Si substrates begin to be introduced to solve this problem. By combining these technologies, Si RF-IC's are moving from R&D stage to the practical use stage.

I. Introduction

Due to the recent and rapid expansion of wireless communication markets such as cellular phones, Si based RF-IC's have been focused as strategic devices for handset industries to realize low production cost and small size terminals [1]-[5]. The main features of Si based RF-IC's for wireless terminals are follows; (1) low production cost comparing with GaAs-IC's especially for very large number mass production, (2) feasibility of system on a chip or single transceiver chip which enable to realize ultra-small size terminals.

In terms of (1) low production cost, chip cost is several times lower than GaAs-IC's, but it depends on the volume of production and the wafer size. In general cases, since Si RF-IC's need the latest Si process, the minimum production number of IC's is very large due to its large wafer size. As the results, Si RF-IC's are suitable for large-scale production such as mobile communication terminals. Recent years, ultra-fine CMOS process [6] and novel SiGe process [7] have been developed. These latest processes enable Si based transistors to have applicable RF performances for mobile communication terminals. In section II, the technological trend of Si RF-IC's is reviewed, and the recent RF performance improvements of transistors based on process technologies is also described.

In terms of (2) system on a chip or single transceiver chip, as long as we use the wafer process based on conventional Si -CMOS or Bipolar or BiCMOS process, RF-IC's can be integrated with CMOS logic / control or Phase Lock Loop (PLL) or analog base band / IF circuit blocks. Even in the case of SiGe, since novel SiGe process has been developed as the extension of present Si bipolar process, it is quite easy to integrate SiGe RF circuits with other conventional Si bipolar / CMOS circuits. To realize single transceiver chip, almost all RF sections must be integrated, therefore low loss inter-stage matching circuits or bias circuits must be fabricated on Si chip. Since CMOS or SiGe processes need to use low resistivity Si substrates, on-chip RF passive circuits for matching / bias circuits are lossy due to dielectric loss of low resistivity Si substrates [1]. In section III, it is shown that the use of high resistivity Si substrates is one of the solutions to realize low loss on-chip RF passive circuits of single transceiver chip.

By combining latest transistor technologies, i.e. CMOS and/or SiGe, and the use of high resistivity Si substrates, Si based RF-IC's will be the strategic devices to realize low cost ultra-small terminals for mobile communication systems.

II. Trend of Si RF-IC's and Transistor Developments

In the middle of 1990's, Si RF-IC was recognized as the next generation RF-IC, which would replace the GaAs RF-IC. Fig.1 shows the number of Si based RF-ICs papers presented at the major international microwave conferences (IEEE Mirowave Theory and Techniques Society (MTT-S) International Microwave Symposium and RF-IC symposium). The increment of paper number year by year indicated the R&D activity of Si based RF-IC's. In 1996, BiCMOS-ICs papers were dominant, because Si bipolar junction transistors had the highest cut-off frequency among Si based transistors. Since 1996, BiCMOS papers have relatively decreased and CMOS and
SiGe papers have rapidly come up. The recent progress of sub-micron CMOS FET process and the development of SiGe HBT have led the technological trend of Si RF-IC’s.

In the case of CMOS, the gate length becomes less than 0.35 μm and the n type MOS FET shows the cut-off frequency beyond 20GHz. Fig.2 shows the cut-off frequency (ft) and d.c. supply voltage (Vdd) of IC’s versus the gate length of CMOS FET’s [6], [8]-[11]. Below 0.35 μm region, ft of CMOS FET exceeds that of conventional Si bipolar junction transistor (BJT), therefore CMOS has been focused as post-GaAs. At present, CMOS design rule for commercial use is around 0.1-0.2 μm and ft is enough for the applications of below 5GHz-band wireless terminals. But from the view point of RF power handling capability, Vdd of below 1.5V is not adequate value even for the receiver use.

In the case of SiGe HBT, ft of over 100GHz has been reported and the breakdown voltage is higher than 0.1-0.2 μm CMOS FET’s. Therefore SiGe HBT’s have attractive features for RF circuits designers.

III. Si RF-IC Technologies to Realize Single Chip Transceiver

Low loss on-chip passive circuit is the key technology to realize single chip transceiver, which has fully compatibility with GaAs-MMIC. Especially for the wireless applications at high frequency range (over 3 GHz), on-chip passive circuit is strongly desired, because the self resonant frequencies of conventional chip inductors are around 2-5GHz. In terms of low production cost and feasibility of system on a chip, Si RF-IC’s have been fabricated on low resistivity Si substrates widely used for conventional Si-IC’s. Therefore the loss of on-chip passive circuits, especially on-chip inductors, is quite high due to the dielectric loss of the Si substrates [1].

In this section, two loss reduction ways are described with referring simulated results of electro-magnetic analysis. One is the use of coplanar wave guide (CPW) structure [1]. In comparison with microstrip line (MS) structure, both simulated and measured CPW type transmission line has lower loss than MS type. Another is the use of other type Si substrate, such as high resistivity Si substrate [12] or SOI substrate [13]. By using these substrates, effect of dielectric loss of the substrate can be reduced.

In order to discuss the loss of transmission lines on various Si substrates, characteristics comparison between six transmission line configurations has been carried out by using electro-magnetic simulation.

(i) MS structure on semi-insulated (ρ =1M Ω : this is an ideal model and is almost same as GaAs-MMIC) substrate.
(ii) MS structure on low resistivity (ρ=50Ω*) substrate.
(iii) MS structure on SOI substrate. (Bulk: ρ=50Ω*)
(iv) MS structure on high resistivity (ρ =1k Ω) substrate.
(v) CPW structure on low resistivity substrate.
(vi) CPW structure on high resistivity substrate.

Cross sectional views of the transmission lines are shown in Fig.3. To make comparison simple, substrate thickness was 400μm and strip line width (W) was 30μm. For CPW transmission line, gap between strip line and grounded metals (S) was designed as 20 μm to obtain 50 Ω characteristic impedance. Table 1 shows the conditions of each transmission lines, and Table 2 shows electro-magnetic simulation results of transmission lines (i)-(vi). Cross sectional views of calculated electrical field distributions are shown in Fig.4.
Fig. 3 Cross sectional views of various transmission lines for electromagnetic simulation.

Table 1 Conditions of various transmission lines.

<table>
<thead>
<tr>
<th>Substrate</th>
<th>MS structure</th>
<th>CPW structure</th>
</tr>
</thead>
<tbody>
<tr>
<td>Semi-insulated substrate</td>
<td>(ρ=1MΩcm⁻¹)</td>
<td>(i)</td>
</tr>
<tr>
<td>Low resistivity substrate</td>
<td>(ρ=50Ωcm⁻¹)</td>
<td>(ii)</td>
</tr>
<tr>
<td>SOI substrate (low resistivity Si)</td>
<td>(ρ=50Ωcm⁻¹)</td>
<td>(iii)</td>
</tr>
<tr>
<td>High resistivity substrate</td>
<td>(ρ=1kΩcm)</td>
<td>(iv)</td>
</tr>
<tr>
<td>(GND)</td>
<td></td>
<td>(vi)</td>
</tr>
</tbody>
</table>

*: ideal model, almost same as GaAs-MMIC.
**: extracted value at 2GHz. At d.c., ρ=10-20Ωcm.

Table 2 Electro-magnetic simulation results of transmission lines (i)-(vi)

| Type     | Transmission line structure | Si substrate          | Resistivity ρ (Ωcm) | Loss (dB/mm) | Z0 (Ω) | 1/n|g |
|----------|-----------------------------|-----------------------|---------------------|--------------|--------|----|
| (i)      | Microstrip line             | Semi-insulated (GaAs compatible) | 10⁶                 | 0.03         | 112    | 2.7|
| (ii)     | Low resistivity             | 50                    | 0.54                | 78           | 3.2    |
| (iii)    | SOI                         | 50                    | 0.55                | 80           | 3.2    |
| (iv)     | High resistivity            | 10³                   | 0.05                | 112          | 2.7    |
| (v)      | Coplanar waveguide          | Low resistivity       | 50                  | 0.33         | 43     | 2.9|
| (vi)     | High resistivity            | 10³                   | 0.05                | 55           | 2.3    |

(CPW is very easy to realize characteristic impedance of 50Ω.)
Table 3 Comparison between calculated and measured results of transmission lines.

<table>
<thead>
<tr>
<th>Type</th>
<th>Transmission line structure</th>
<th>Si substrate</th>
<th>Loss (dB/mm)</th>
<th>$\lambda_0/\lambda_g$</th>
</tr>
</thead>
<tbody>
<tr>
<td>(ii)</td>
<td>Microstrip line</td>
<td>Low resistivity</td>
<td>0.59 [0.24]</td>
<td>3.5 [3.2]</td>
</tr>
<tr>
<td>(iv)</td>
<td></td>
<td>High resistivity</td>
<td>0.08 [0.05]</td>
<td>2.7 [2.7]</td>
</tr>
<tr>
<td>(v)</td>
<td>Coplanar waveguide</td>
<td>Low resistivity</td>
<td>0.20 [0.33]</td>
<td>3.5 [2.9]</td>
</tr>
</tbody>
</table>

Fig. 4 Cross sectional views of calculated electrical field distributions of various transmission lines.
Case (i) is an ideal case, and the electric field distribution shown in Fig.4(a) is normal. In the case of (ii), since the substrate resistivity is low, the electric field does not come into the substrate sufficiently as shown in Fig.4(b), and equivalent ground plane of MS can not be the backside of substrate but inside of substrate. Therefore, the loss is relatively higher and the characteristic impedance is relatively lower than that of MS line (i) or (iv). In the case of SOI (iii), calculated results are almost same as the case (ii) as shown in Fig.4(c). Difference of transmission characteristics between (i) and (iv) is fairly small, and high resistivity Si substrate can be used instead of GaAs like semi-insulated substrate as shown in Fig.4(d). As the results, the use of high resistivity substrate is quite effective way to reduce the loss of transmission line on Si substrate.

In the case of CPW (v), since the electrical field is concentrated at the gap between strip line and grounded metals as shown in Fig.4(e), it does not go into the lossy substrate deeply and the CPW (v) has 50% lower loss than that of MS (ii). The use of CPW structure instead of MS is effective for the loss reduction of passive circuits on low resistivity Si substrate. To evaluate the results, two types of transmission lines (MS (ii) and CPW (v)) are fabricated and measured. Measured results are shown in Table 3, and are in agreement with the simulated results shown in Table 2. Even in the case of CPW on high resistivity Si substrate (vi), its loss is not exceeded that of MS (iv) on the same resistivity substrate. Then CPW structure can be usable. In both cases, (v) and (vi), there are grounded plane existed on the backside of the substrate, but they don't affect the transmission line characteristics. Therefore, transmission lines (v) and (vi) can be considered as CPW.

As the results, the use of CPW structure is one of the effective ways to reduce the loss of passive circuits on low resistivity Si substrate. But, to reduce the loss to the GaAs-MMICs level, high resistivity Si have to be used.

Accordingly, it is shown that the use of high resistivity Si substrate is effective way to reduce the loss of on-chip passive circuits. Based on this result, 5.8GHz-band on-chip matching LNA is developed by using high resistivity Si substrate.

The schematic diagram of the fabricated LNA is shown in Fig.5. The emitter size of BJT is 0.8 x 72μm^2. The input port is NF matched and the output port is gain matched to 50Ω using the CPW type spiral inductors. A photograph of the fabricated LNA is shown in Fig.6. The chip size is 1mm x 1.2mm.

Fig. 7 shows the measured frequency dependence of gain and NF of the LNA's fabricated on both low and high resistivity Si substrates. The gain of 6.9dB and NF of 3.3dB are obtained for high resistivity, and 5.0dB and 4.2dB respectively for low resistivity, with 3V, 3mA d.c. supply power.

![Schematic diagram of fabricated 5.8GHz on-chip matching LNA](image)

![Photograph of fabricated 5.8GHz on-chip matching LNA](image)

![Measured frequency dependence of gain and NF of the LNA's fabricated on high / low resistivity Si substrates](image)
IV. Conclusion

The latest CMOS fine process and novel SiGe HBT process has led Si RF-IC's to the practical use for mobile communication terminals below 2GHz. To make full use of Si RF-ICs merits, the integration of RF / IF / Base Band circuits is the key issue. For the integration of RF sections, achievement of low-loss on-chip passive circuits is quite important.

In this paper, low-loss on-chip passive circuit techniques are described. One is the use of CPW structure and another is the use of high resistivity Si substrate. Based on the electro-magnetic simulation results, transmission line characteristics are discussed. The use of CPW is effective when low resistivity Si substrate has to be used, and the use of high resistivity Si substrate is quite effective to reduce the loss to the GaAs-MMICs level.

Based on the simulated results, on-chip matching Si-MMIC LNA is fabricated on high resistivity Si substrate and it indicates low loss on-matching characteristics. By combining the latest Si transistor including CMOS FET / SiGe HBT and low-loss on-chip passive circuits on high resistivity Si substrates, Si RF-IC's will be adopted up to 10GHz mobile communication applications.

References


