

April 2, 2019

Introduction to Surface Acoustic Wave (SAW) Devices

Part 7: Basics of RF Circuits

Ken-ya Hashimoto

Chiba University

k.hashimoto@ieee.org

<http://www.te.chiba-u.jp/~ken>

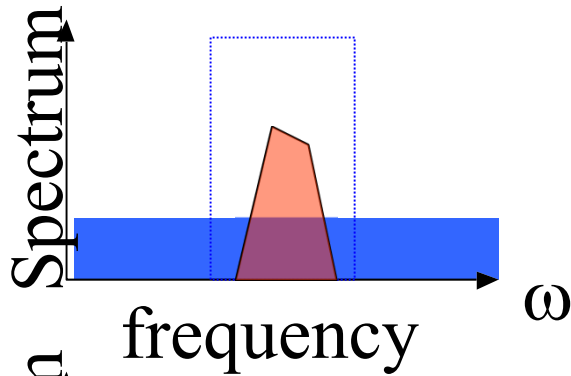
Contents

- Noise Figure and Non-Linearities
- RF Amplifiers
- Low Noise Amplifier Design Example

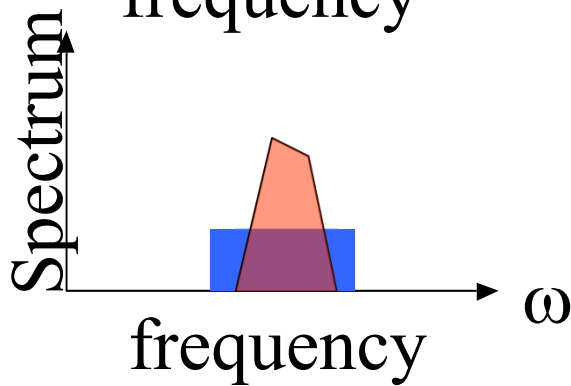
Contents

- Noise Figure and Non-Linearities

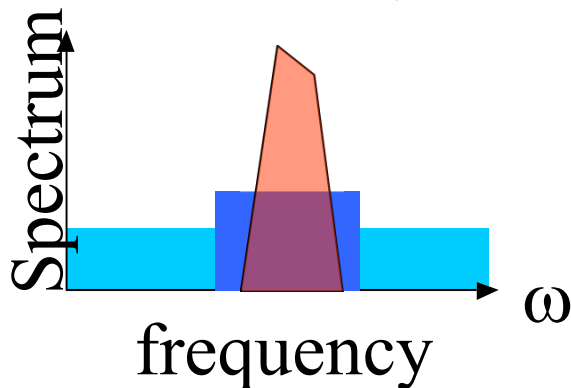
Signal to Noise Ratio (SNR)



(a) Signal + Noise



(b) After Front End Filtering

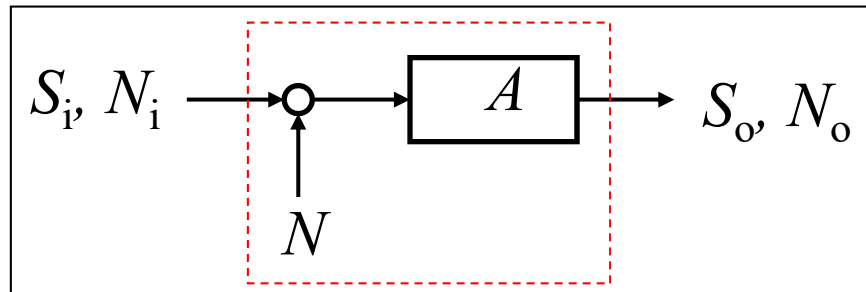


(c) After Front End Amplifying

Noise Figure, NF

$$F = \frac{S_i / N_i}{S_o / N_o} = 1 + \frac{N}{N_i} \quad [\text{Power Ratio}]$$

$$NF = 10 \log F$$



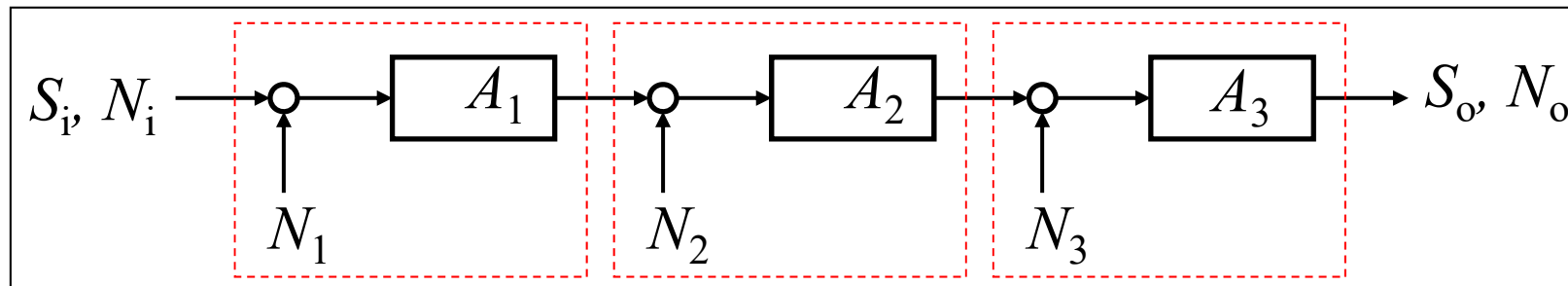
N_i : Input Noise Power

N_o : Output Noise Power

N : Thermal Noise

A : Power Gain

Cascade Connection



$$P_{\text{output}} = A_3 (A_2 (A_1 (S_i + N_i + N_1) + N_2) + N_3)$$

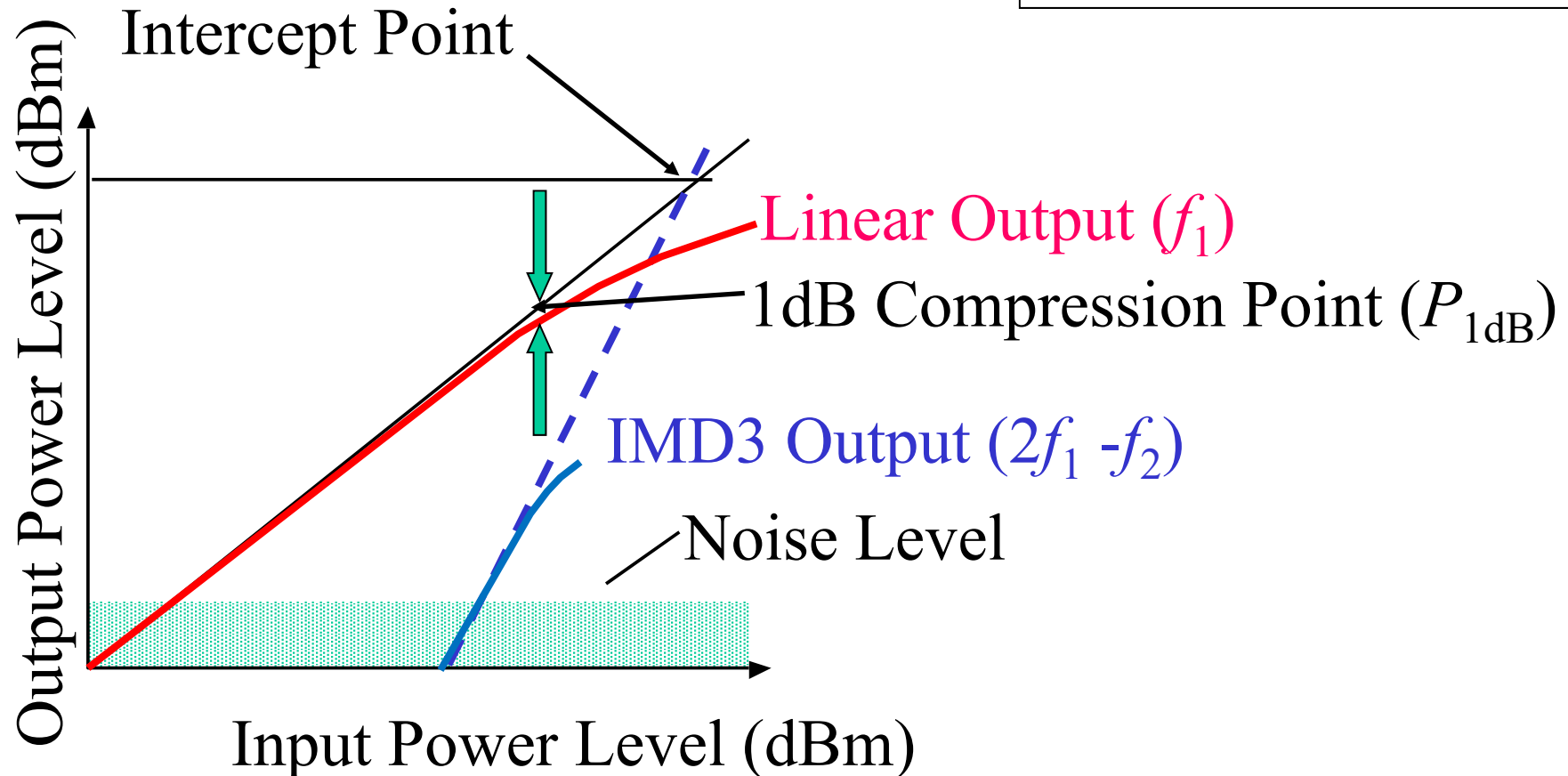
$$F = 1 + \frac{N_1}{N_i} + \frac{N_2}{N_i A_1} + \frac{N_3}{N_i A_1 A_2} = F_1 + \frac{F_2 - 1}{A_1} + \frac{F_3 - 1}{A_1 A_2}$$

Most Significant!

3rd order Intercept Point (IP3)

Generation of Jammer signals by
Intermodulation

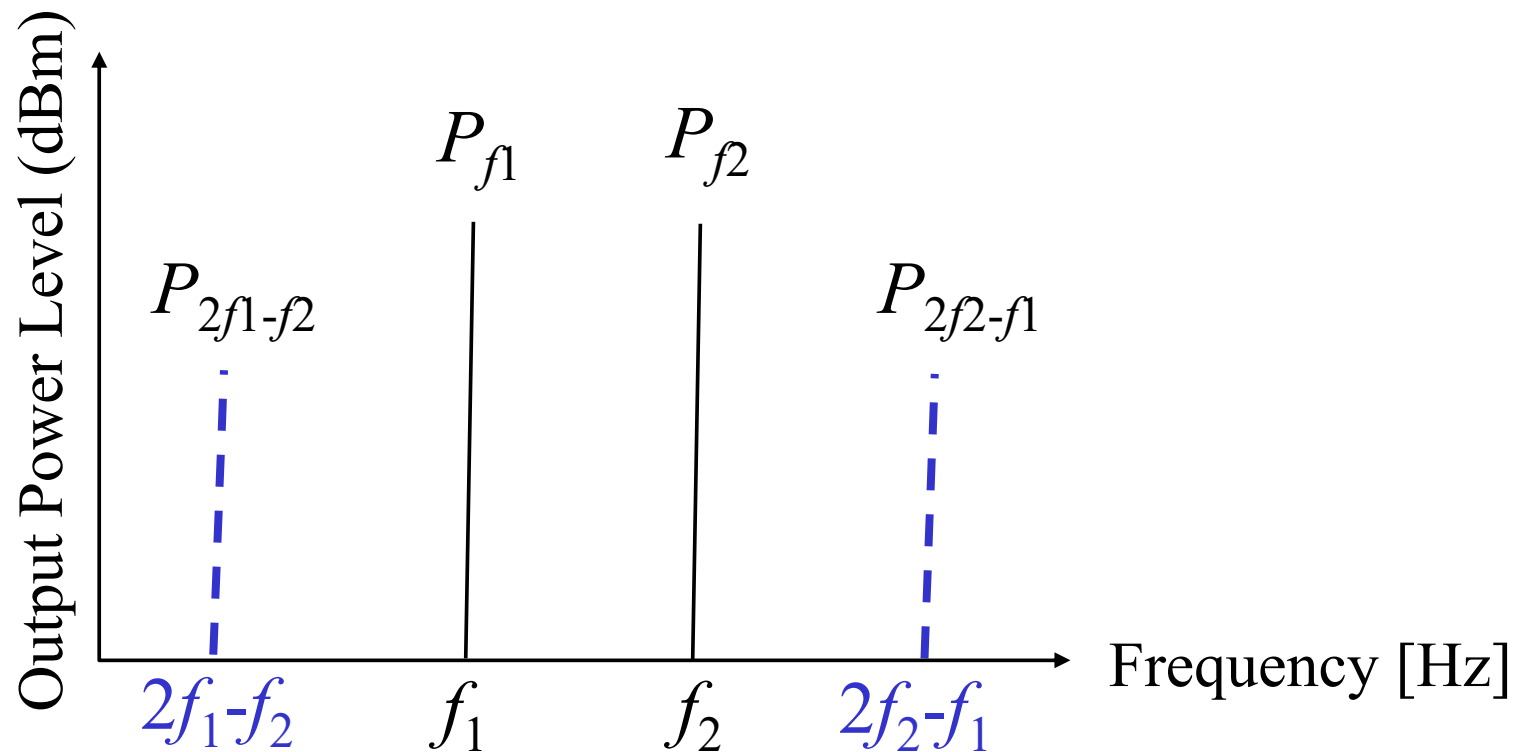
$$\text{IIP3} \approx P_{1\text{dB}} + 9.6 \text{ [dB]}$$



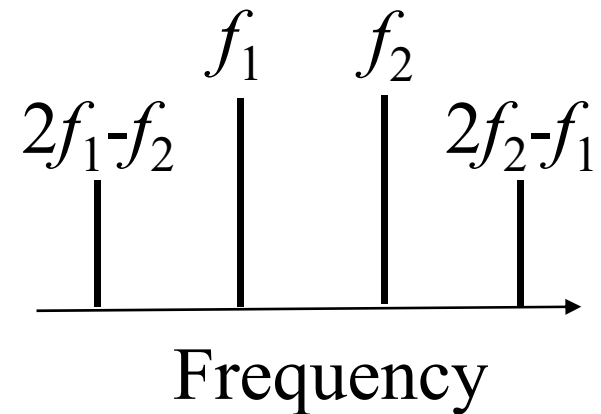
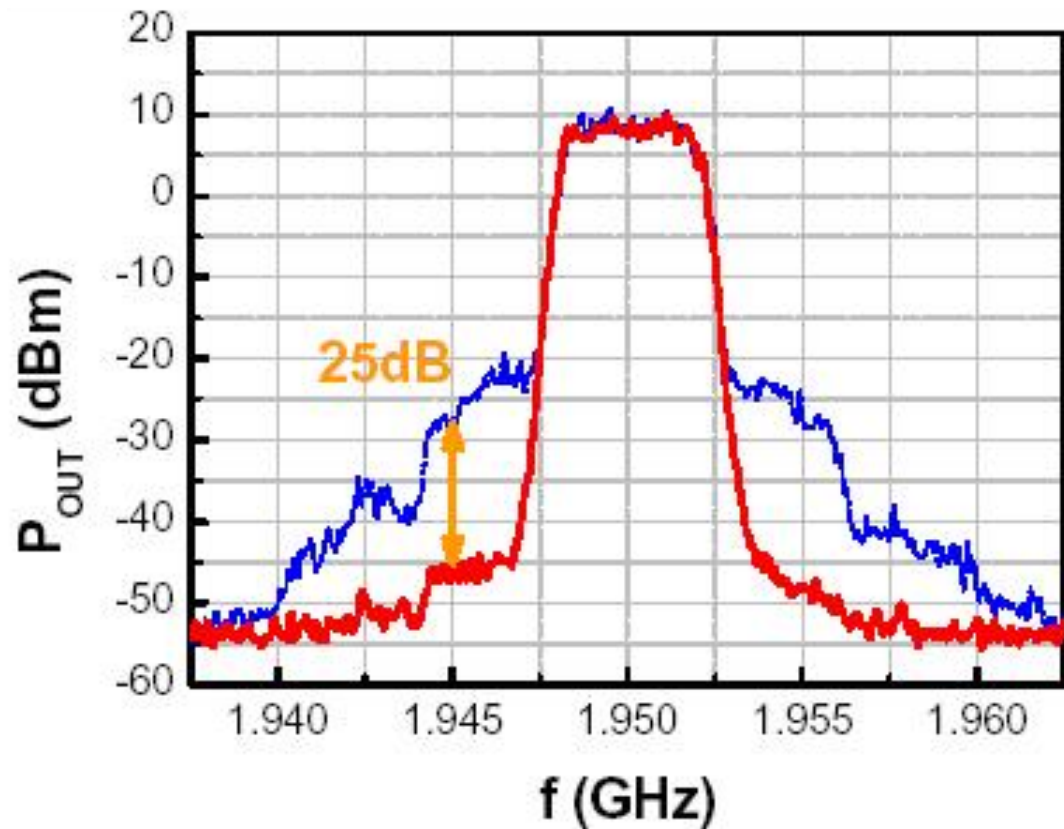
3rd order Intercept Point (IP3)

$$P_{2f_1-f_2} [\text{dBm}] = 2P_{f_1} [\text{dBm}] + P_{f_2} [\text{dBm}] - 2 \times \text{IP3} [\text{dBm}]$$

$$P_{2f_2-f_1} [\text{dBm}] = 2P_{f_2} [\text{dBm}] + P_{f_1} [\text{dBm}] - 2 \times \text{IP3} [\text{dBm}]$$



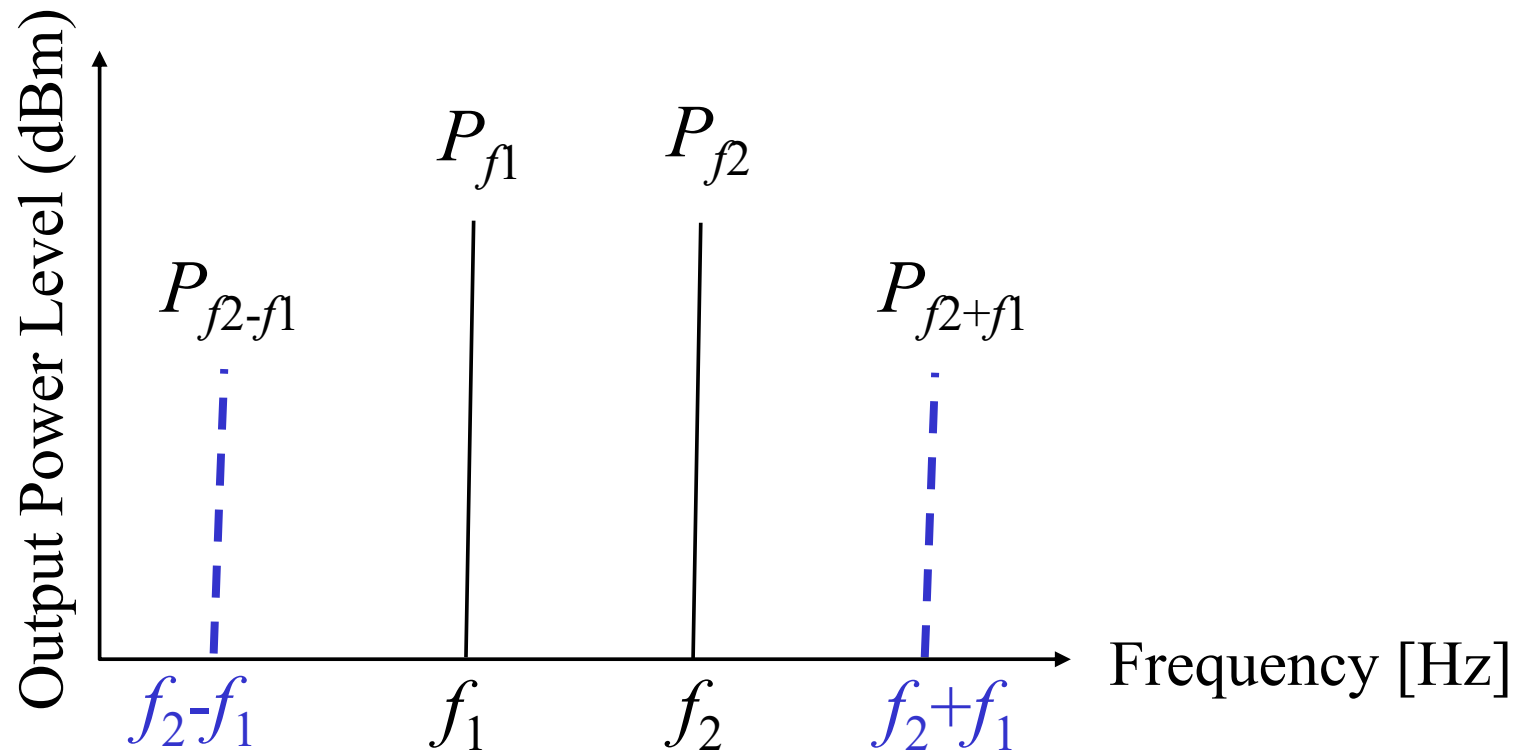
Spectrum Regrowth in PA and DPX = Self Mixing of Tx Signals



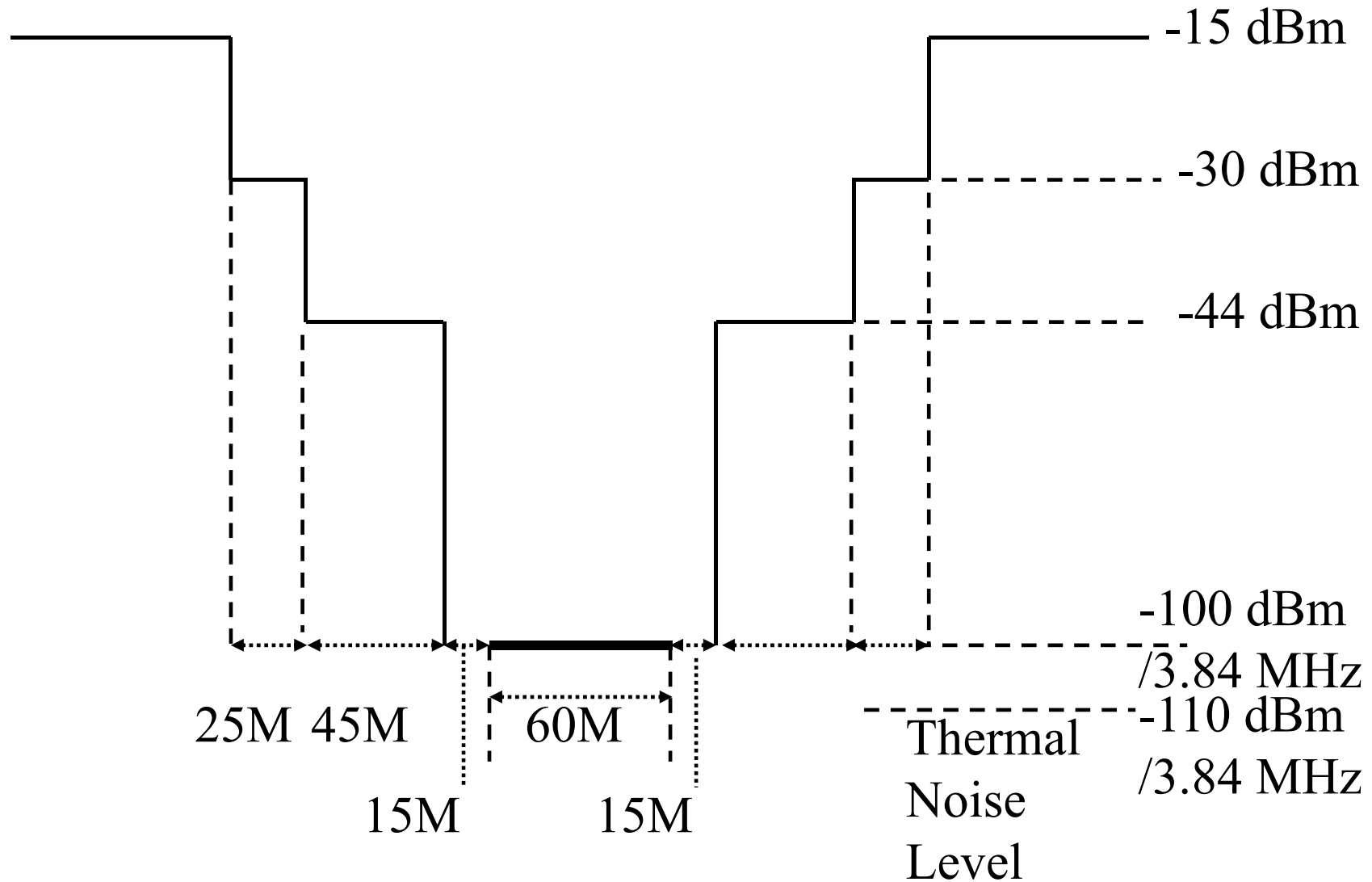
Jammer Signal Emission to Adjacent Channels

2nd order Intercept Point (IP2)

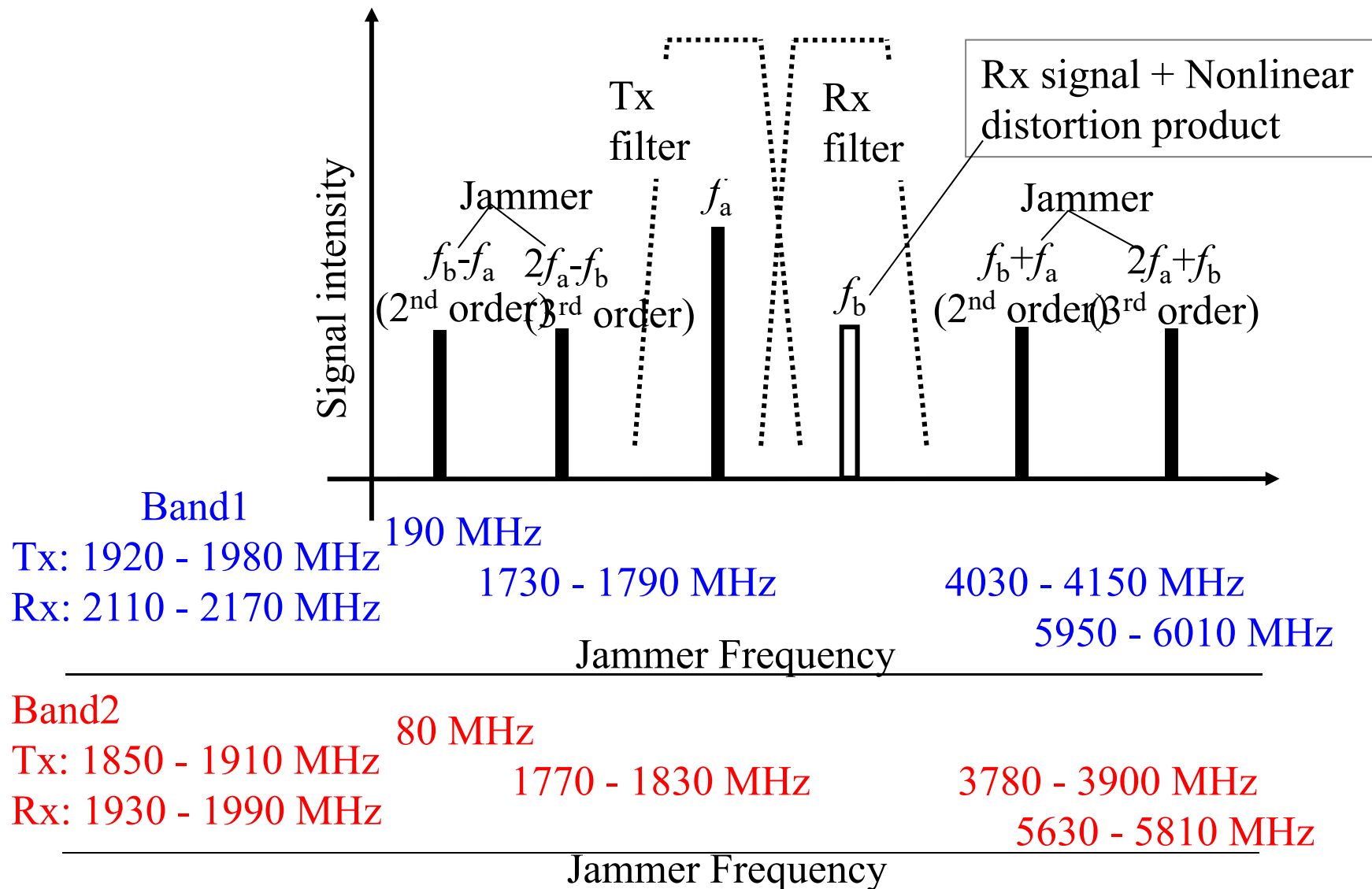
$$P_{f_2 \pm f_1} [\text{dBm}] = P_{f_2} [\text{dBm}] + P_{f_1} [\text{dBm}] - \text{IP2} [\text{dBm}]$$



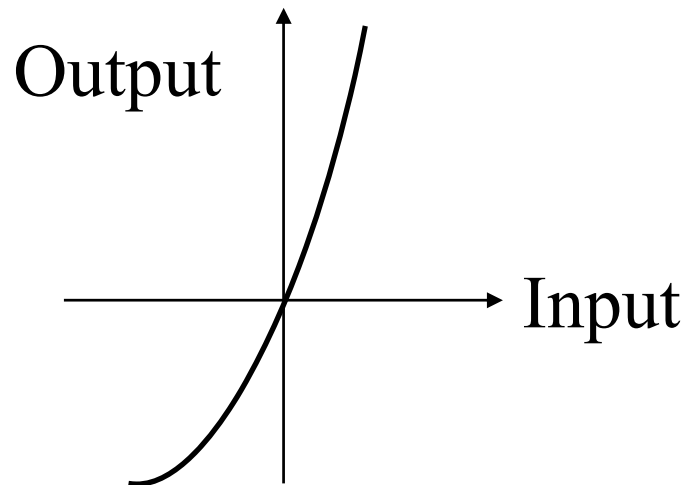
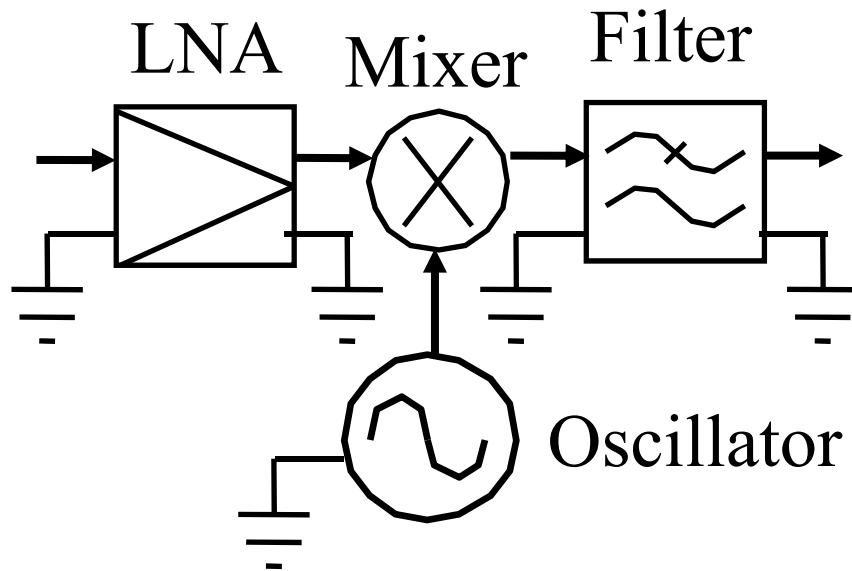
Blocking Test Example (W-CDMA Band II)



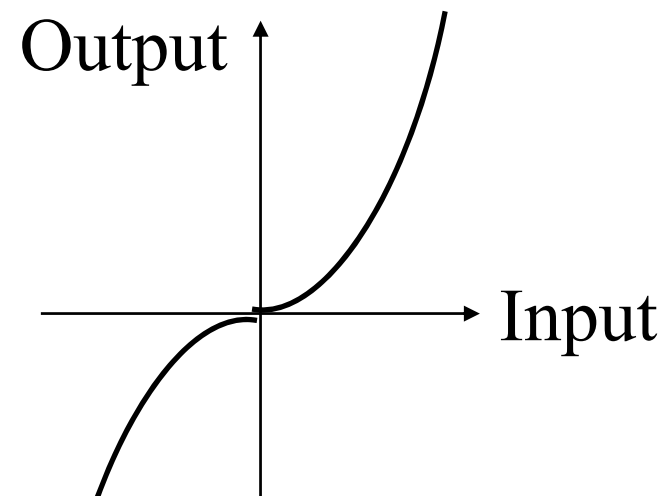
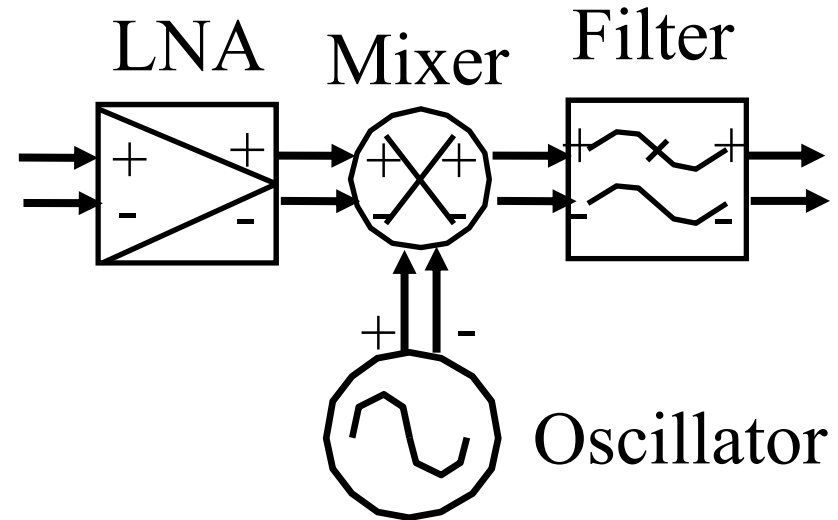
Inter Modulation Distortion in Nonlinear Circuit for WCDMA System



IP2 Suppression by Balanced Topology



Unbalanced Topology

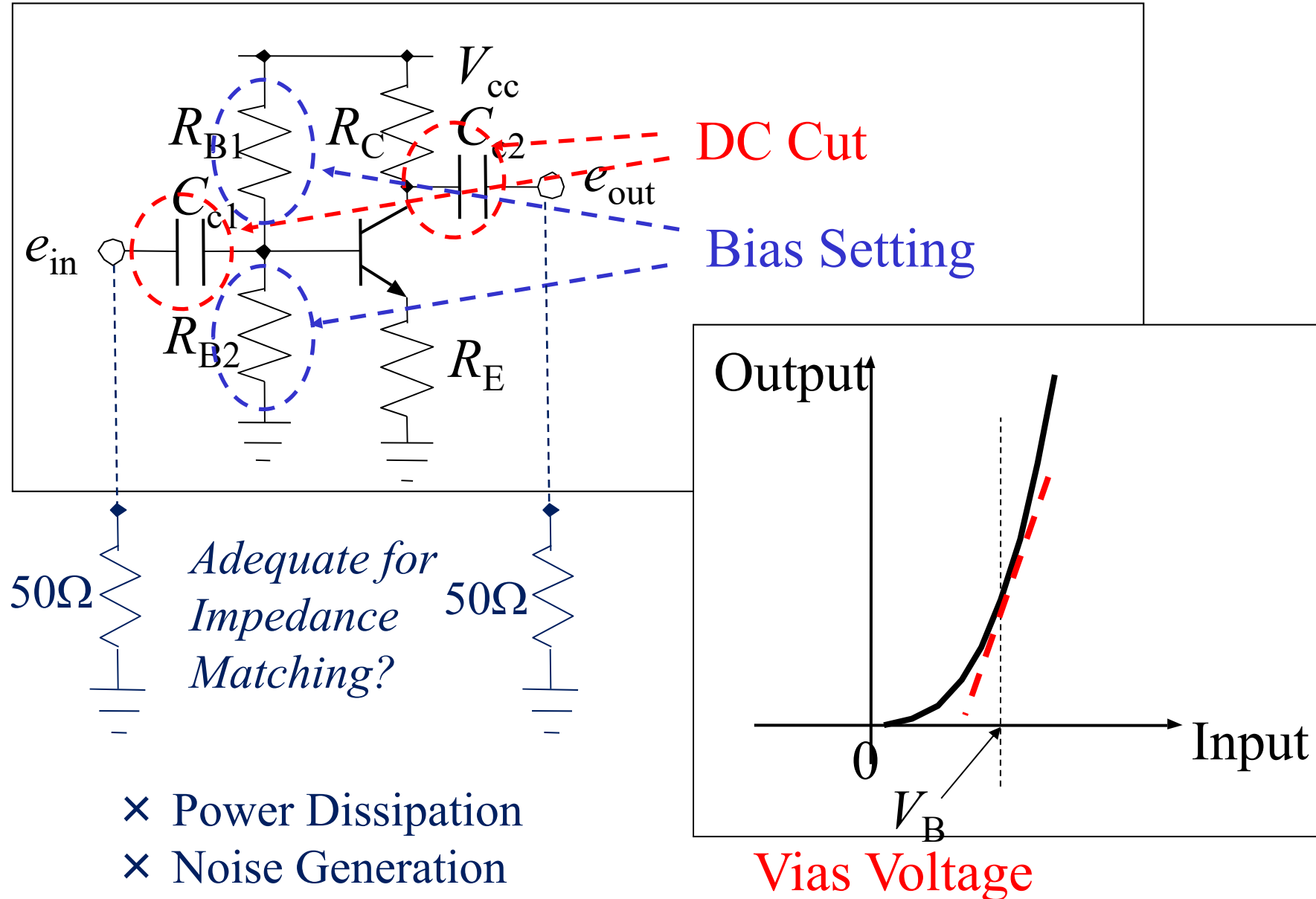


Balanced Topology

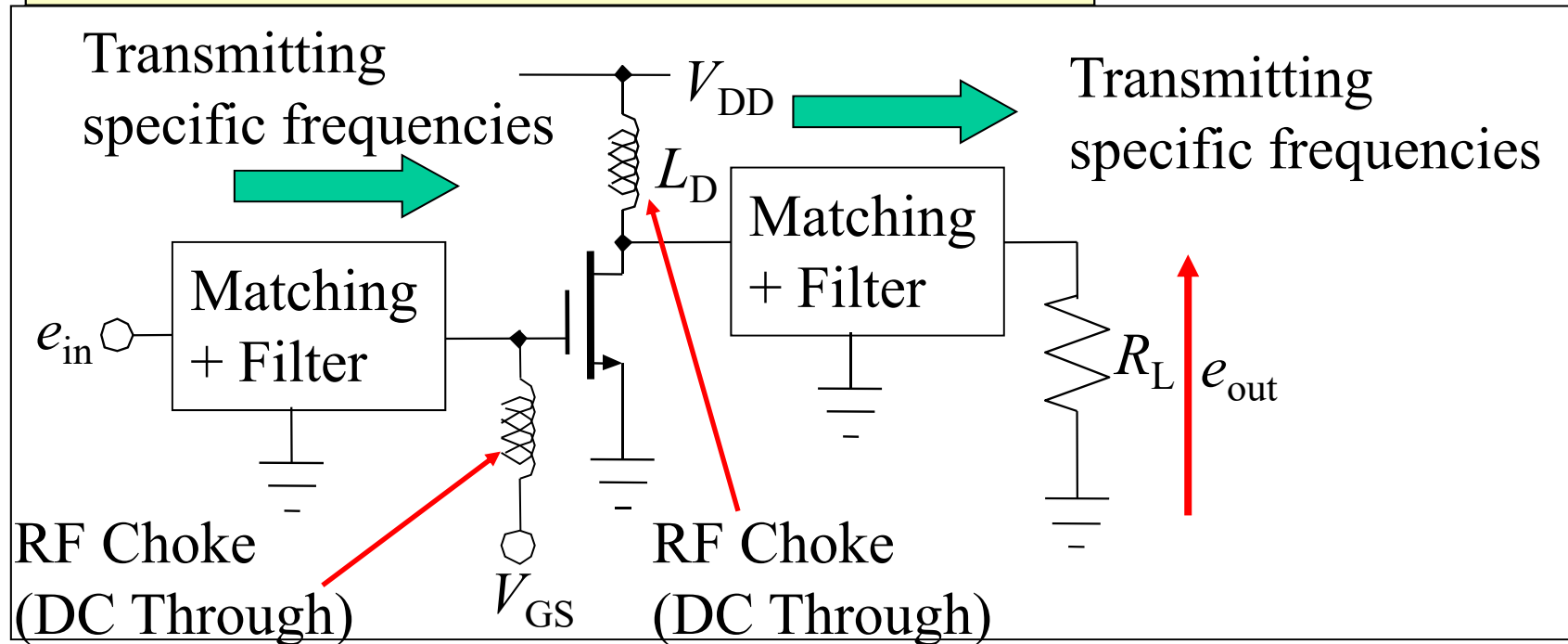
Contents

- RF Amplifier

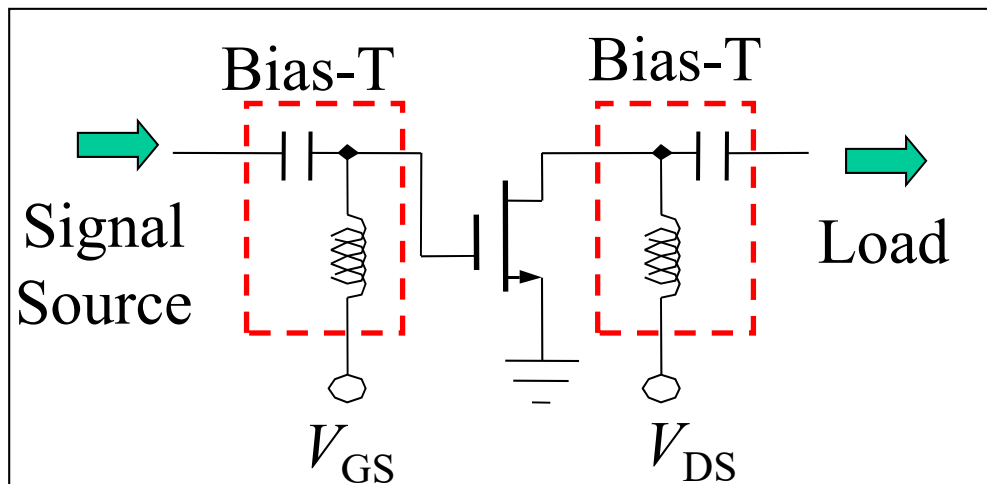
Capacitor Coupled LF Amplifier



RF Amplifier Configuration

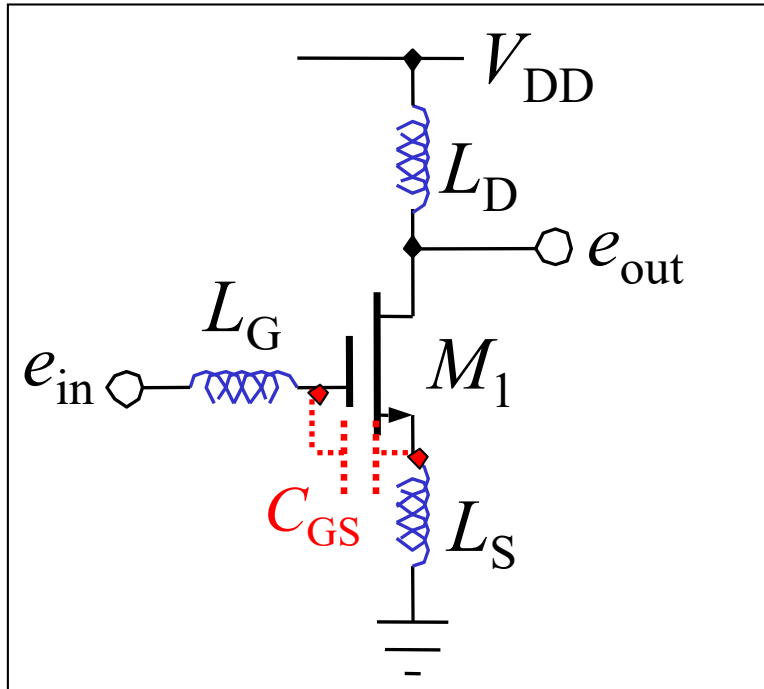


Measurement of Transistor S Parameters



Small Signal Measurement
for Given Bias Condition
(For $R_0=50\ \Omega$)

Common Source Amplifier



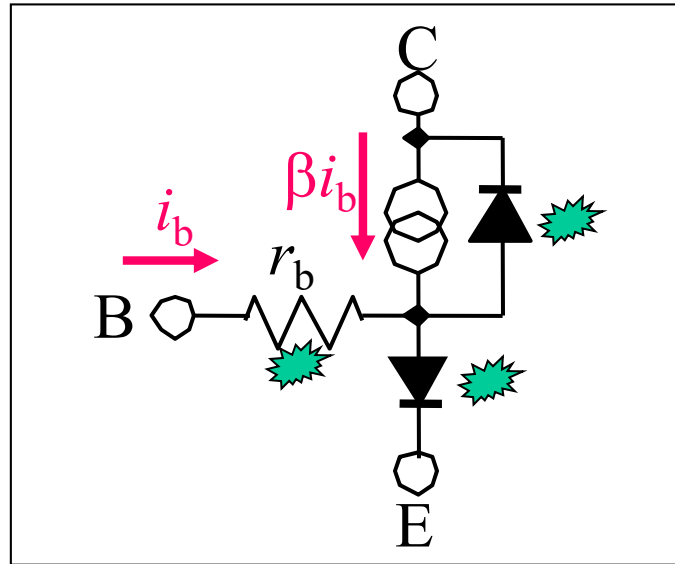
$L_G, L_S \rightarrow$ Impedance Matching

$L_D \rightarrow$ RF Choke

Large Voltage Gain

$$Z_{in} = i\omega L_G + \frac{1}{i\omega C_{GS}} + i\omega L_S \left[1 + \frac{g_m}{i\omega C_{GS}} \right]$$

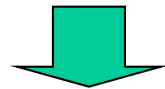
$$= \underbrace{\frac{L_S g_m}{C_{GS}}}_{\rightarrow 50\Omega} + \underbrace{i\omega(L_G + L_S) + \frac{1}{i\omega C_{GS}}}_{\rightarrow 0}$$



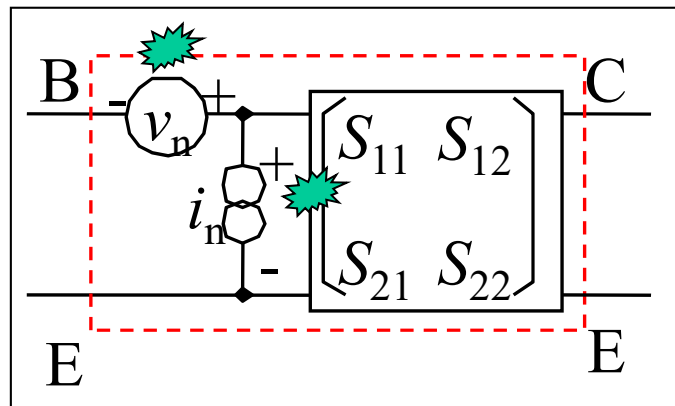
Noise Generation

Thermal Noise (Resistance Origin)

+ Shot Noise (Junction Origin)



Small Signal Model (Linearize)



Input Referred Noise

$$i_n = i_c + i_u$$

i_c : correlated with v_n ($\equiv Y_c v_n$)

i_u : not-correlated with v_n

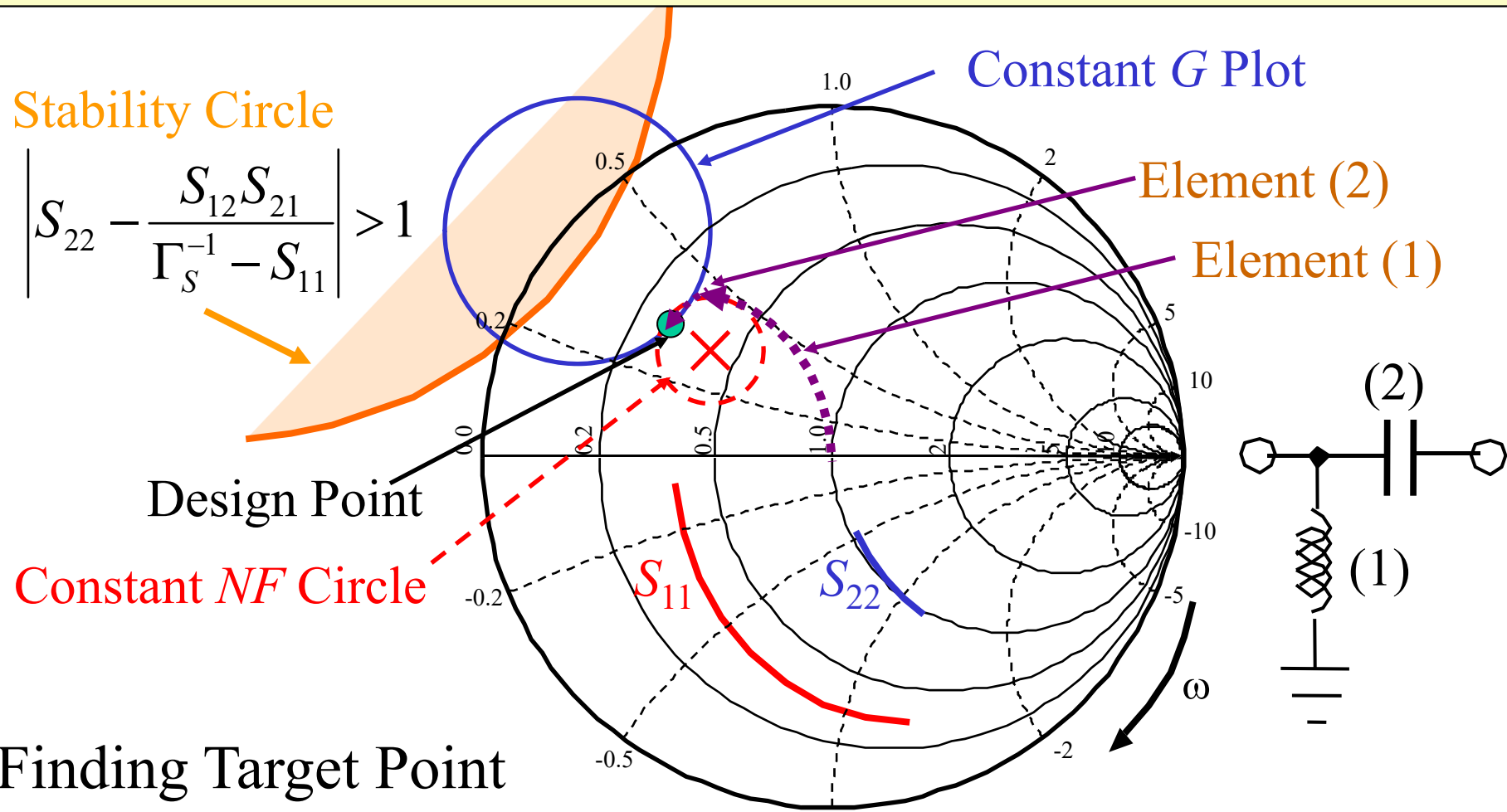
$$\left. \begin{aligned} \overline{v_n^2} &= 4kTB R_n \\ \overline{i_u^2} &= 4kTB G_u \end{aligned} \right\} B: \text{Frequency Bandwidth}$$

Rollet Stability (K) Factor

Unconditionally Stable When $K > 1$

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2 |S_{21}S_{12}|}$$

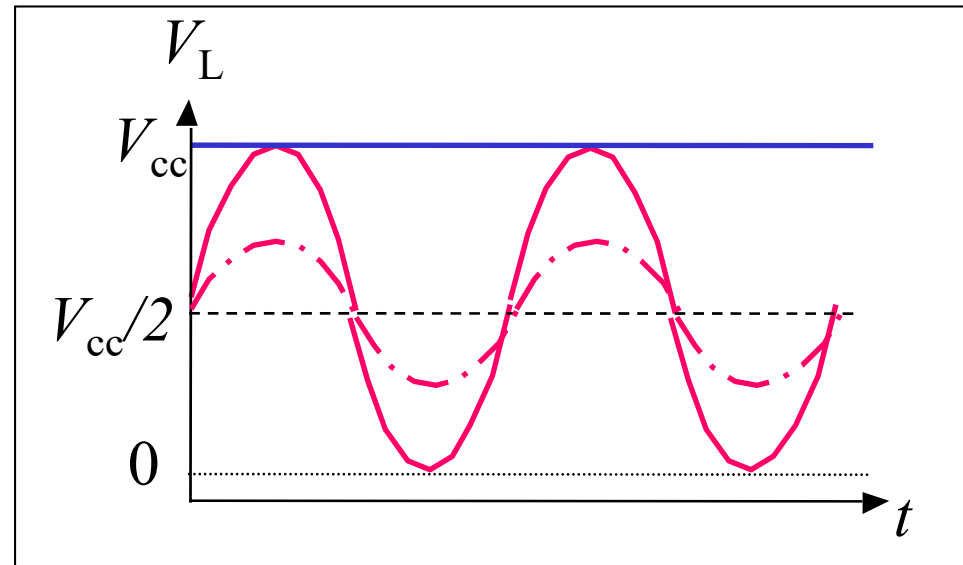
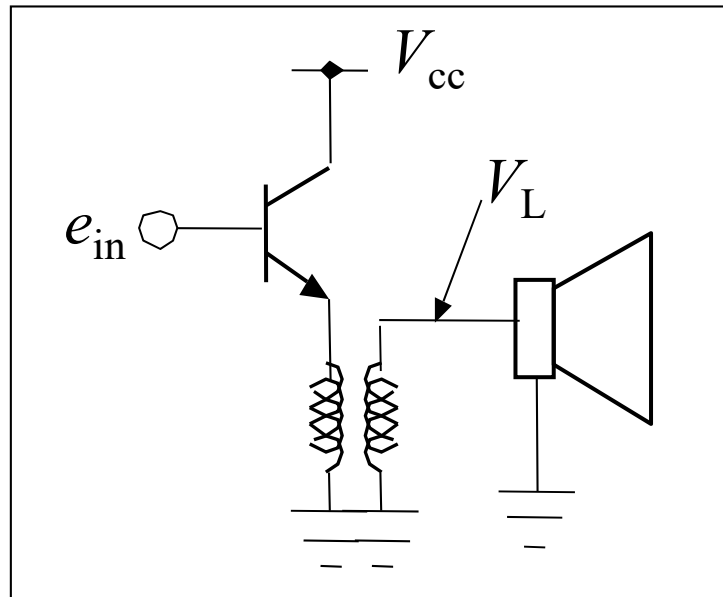
Matching Circuit Design Using Smith Chart



- Finding Target Point
- Designing Input Matching Circuit
- Designing Output Matching Circuit
- Verification (Often S_{11} and S_{22} are NOT acceptable)

Gain and NF are Dependent on Bias Current (Voltage)

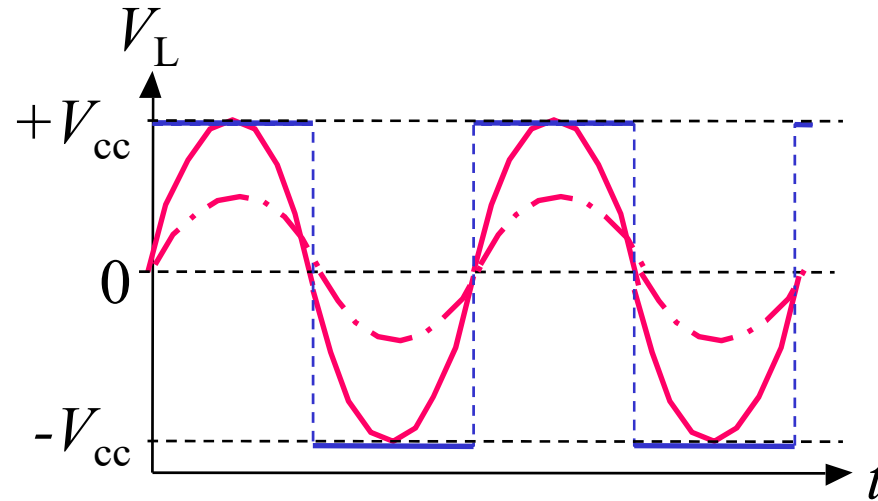
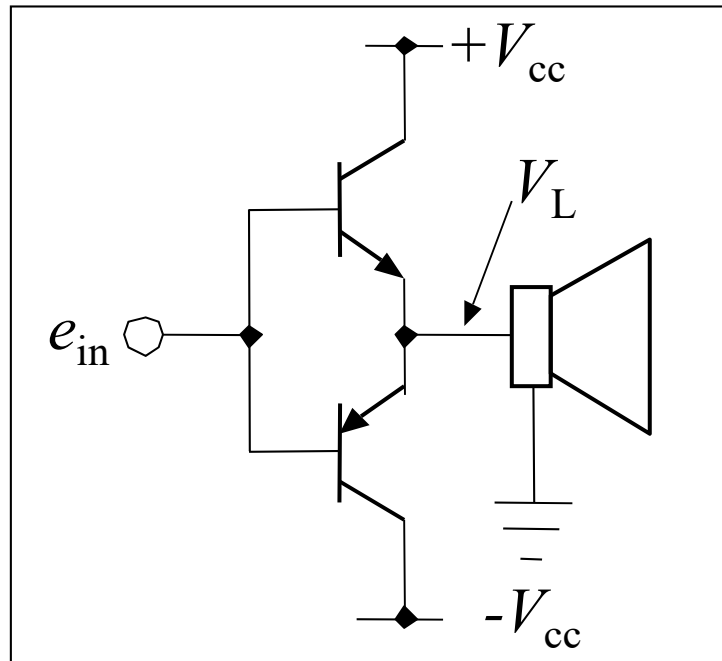
Power Efficiency η of Class A Amplifier



$$\eta = \frac{\frac{1}{R_L} \frac{1}{T} \int_0^T [V_o \sin(2\pi t / T)]^2 dt}{\frac{1}{R_L} \frac{1}{T} \int_0^T V_{cc} \left[\frac{V_{cc}}{2} + V_o \sin(2\pi t / T) \right] dt} = \left[\frac{V_o}{V_{cc}} \right]^2$$

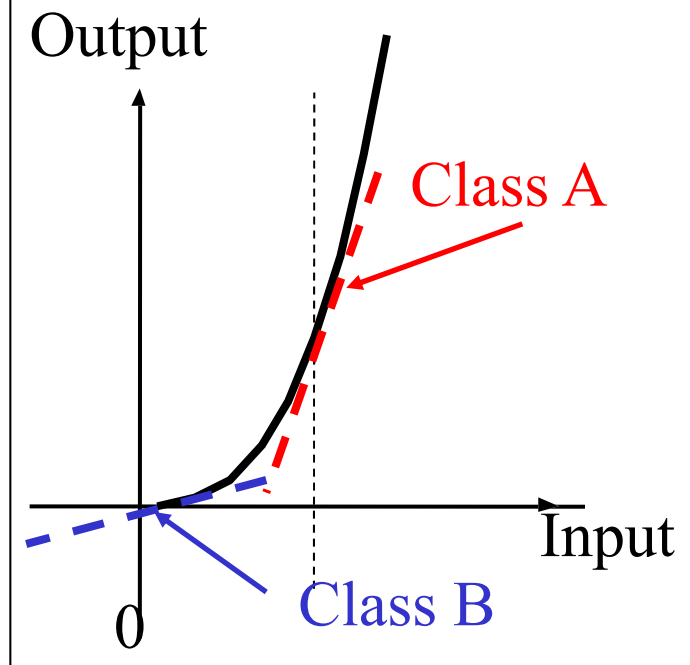
Maximum η 25% (at $V_o = V_{cc}/2$)

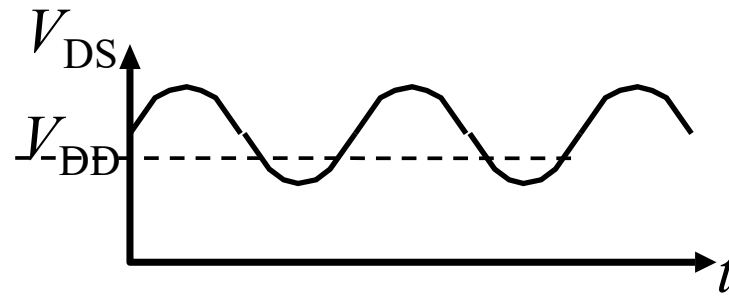
Power Efficiency η of Class B Amplifier



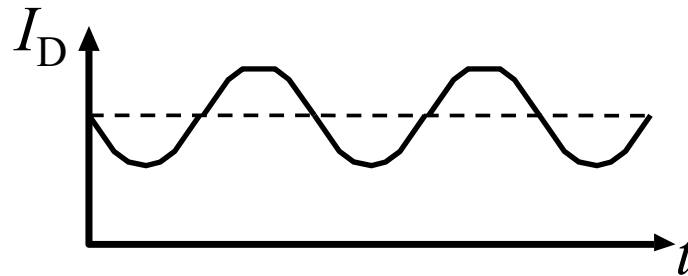
$$\eta = \frac{\frac{1}{R_L} \frac{2}{T} \int_0^{T/2} [V_o \sin(2\pi t / T)]^2 dt}{\frac{1}{R_L} \frac{2}{T} \int_0^{T/2} V_{cc} [V_o \sin(2\pi t / T)] dt} = \frac{\pi}{4} \left[\frac{V_o}{V_{cc}} \right]$$

Maximum η 78.5% (at $V_o = V_{cc}$)

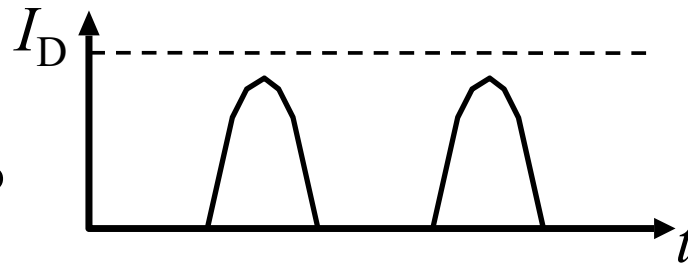




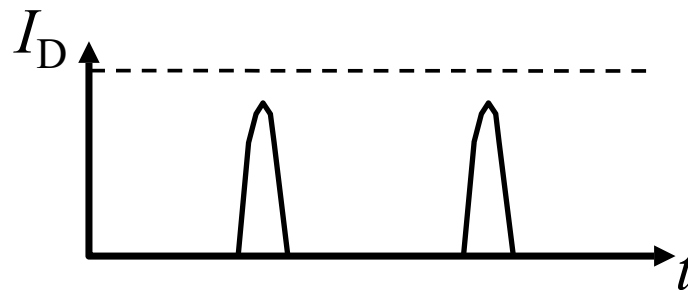
Class A
 $\eta_{\max} = 50\%$
 for RF



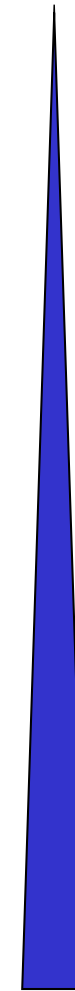
Class B
 $\eta_{\max} = 78.5\%$



Class C
 $\eta_{\max} = 100\%$
 (At $P=0$)



Efficiency Distortion



Good



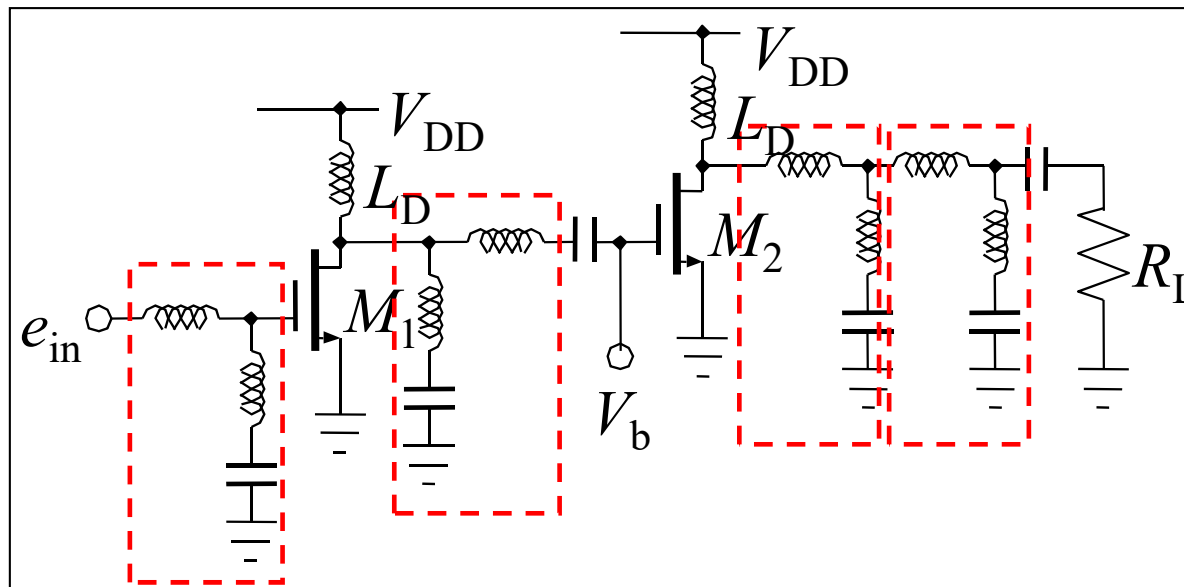
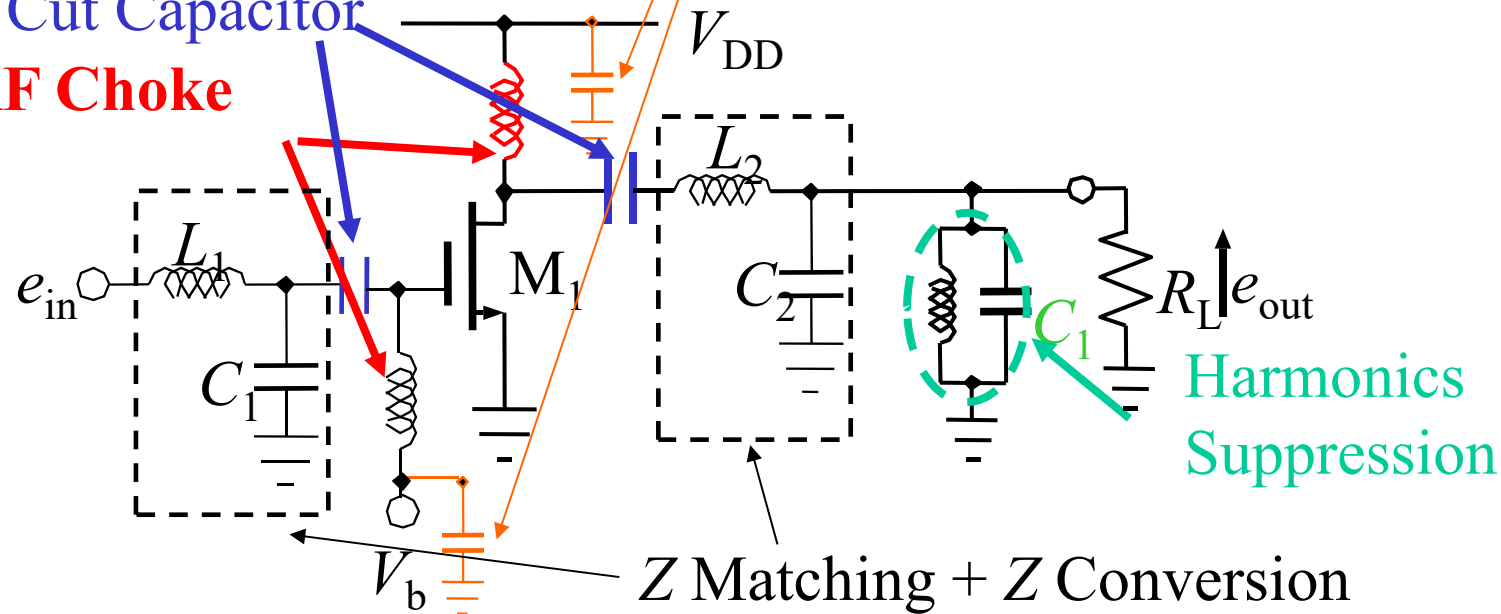
Bad

Power Amplifier

DC Cut Capacitor

RF Choke

Rejecting RF Leakage

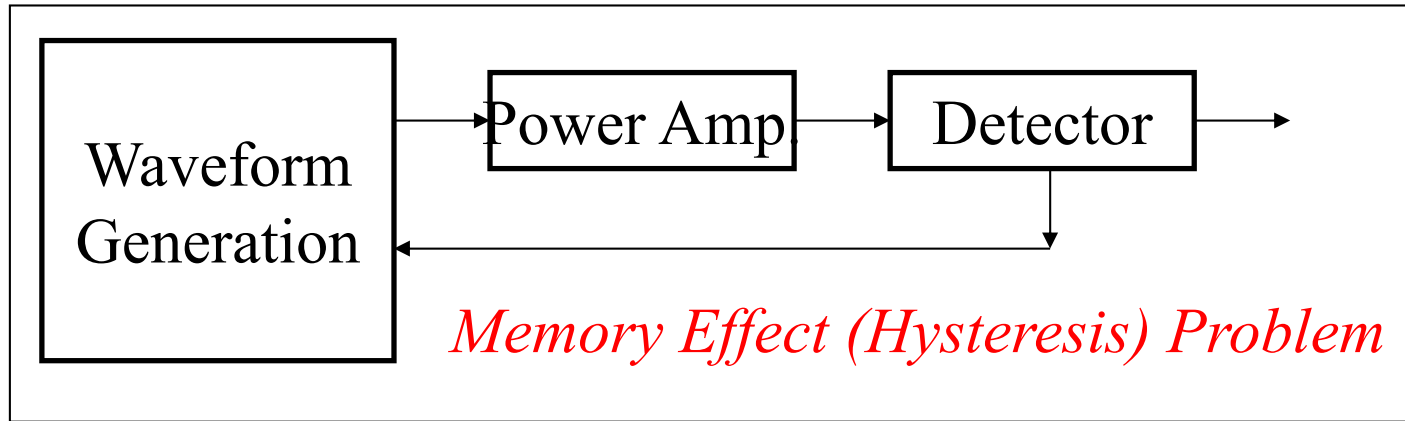


Driver + Main Amplifier

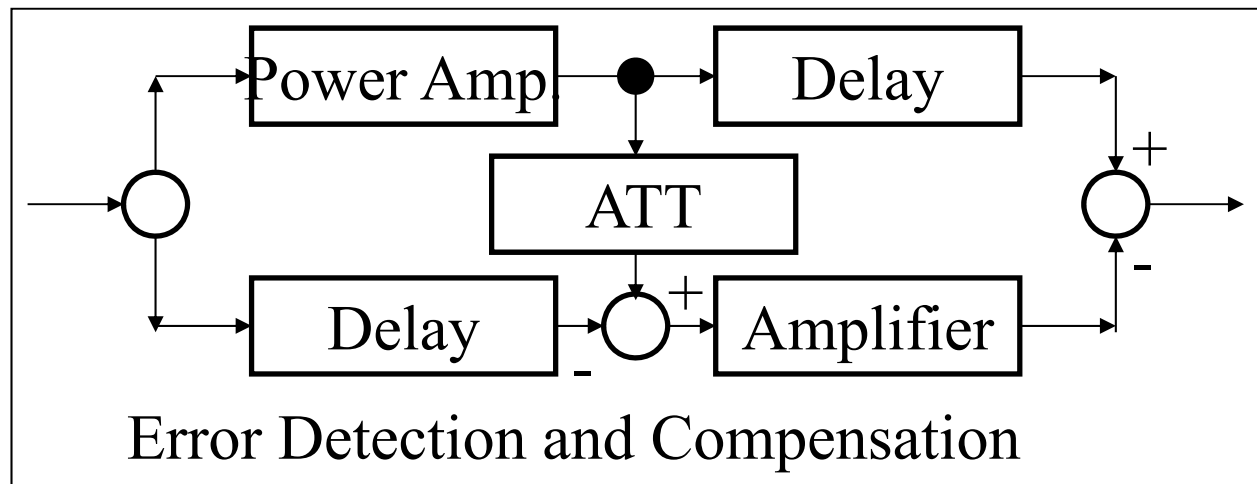
Linear High Efficiency PA

Pre-distortion

Feedback Compensation



Feed-Forward PA



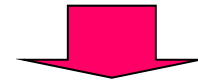
Linear Amplifier with Non-linear Components (LINC)

$$E(t) = A(t) \sin(\omega_c t + \varphi(t))$$

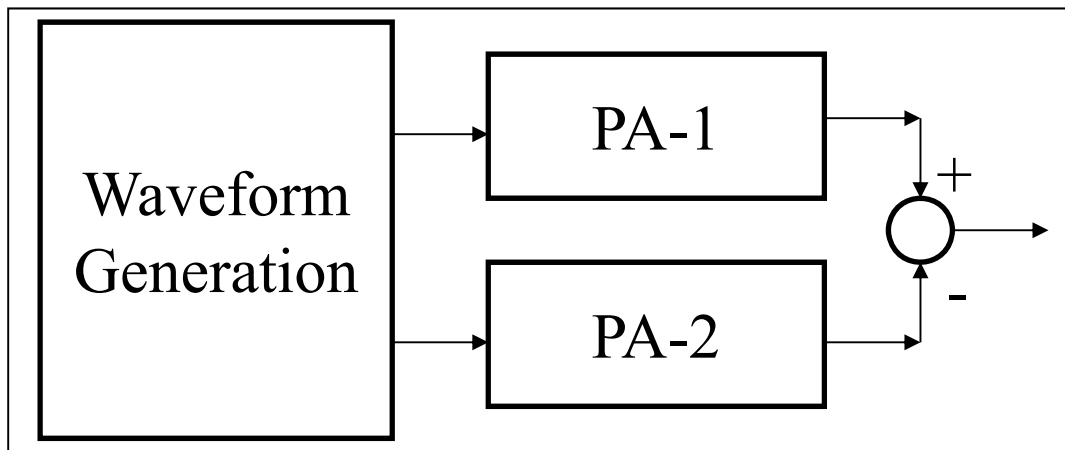
$$= \frac{A_{\max}}{2} [\cos(\omega_c t + \varphi(t) - \theta(t)) - \cos(\omega_c t + \varphi(t) + \theta(t))]$$

where $\theta(t) = \cos^{-1}(A(t)/A_{\max})$

Constant Amplitude



Non-Linear PA Applicable

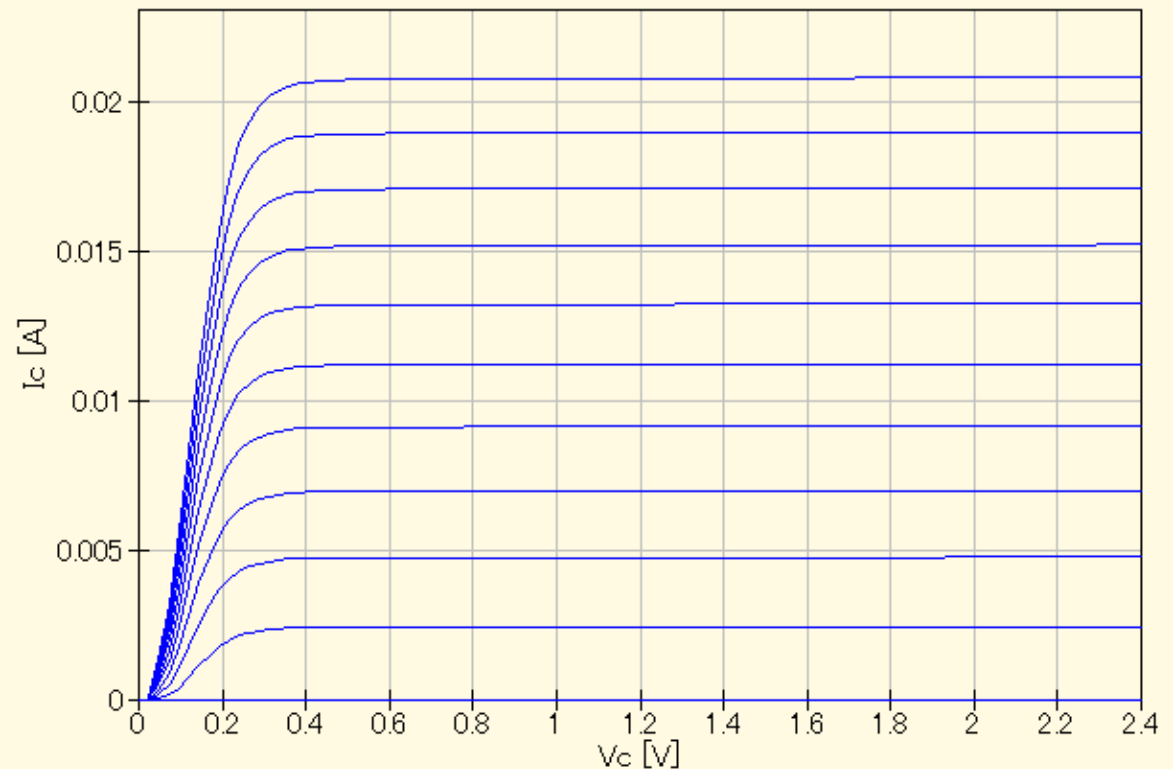
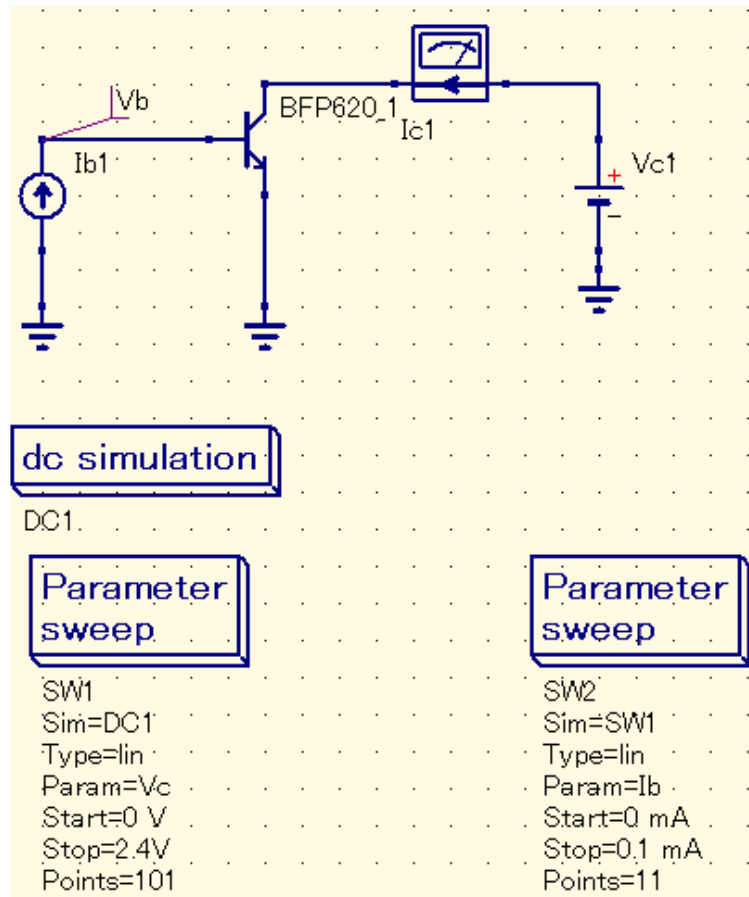


Contents

- Low Noise Amplifier Design Example

Use of High Speed Transistor BFP620

Design Low Noise Amplifier at 2.488 GHz. $V_{cc}=1.5$ V and $I_c=5$ mA. Low NF and Return Suppression Mandatory.
How High Gain Achievable?



Step 1 Bias Circuit Design

Qucs 0.0.15 - Project: RFamp

File Edit Positioning Insert Project Tools Simulation View Help

Simulate F2
View Data Display/Schematic F4
Calculate DC bias F8
Show Last Messages F5
Show Last Netlist F6

Content of 'RFamp'

- Schematics
 - test.sch
 - schematic1.sch
 - schamtic2.sch
 - exer8.sch
 - exer7.sch
 - exer5.sch
 - exer4.sch
 - exer3.sch
 - exer2.sch
 - exer1.sch**
 - exer0.sch
 - design1.sch
 - baseAmp.sch
- VHDL
- Verilog
- Data Displays
- Datasets
- Others

Schematic Diagram:

The circuit diagram shows a BFP620_1 transistor in a common-emitter configuration. The base is biased using a voltage divider consisting of a 30k Ohm resistor (R1) and a 1 Ohm resistor (R2) connected to a 1.5V DC source (V1). The emitter is connected to ground through a 20 pF capacitor (C2). The collector is connected to a 100 nH inductor (L1) and a 20 pF capacitor (C1). The output is taken from the collector through a 50 Ohm load (VP2). The input is connected to a 50 Ohm source (VP1). The simulation results show the DC bias voltages: 1.49474V at the base, 0.834519V at the emitter, and 1.49474V at the collector.

Simulation Results:

S parameter simulation

SP1
Type=lin
Start=0.5 GHz
Stop=5.5 GHz
Points=2001

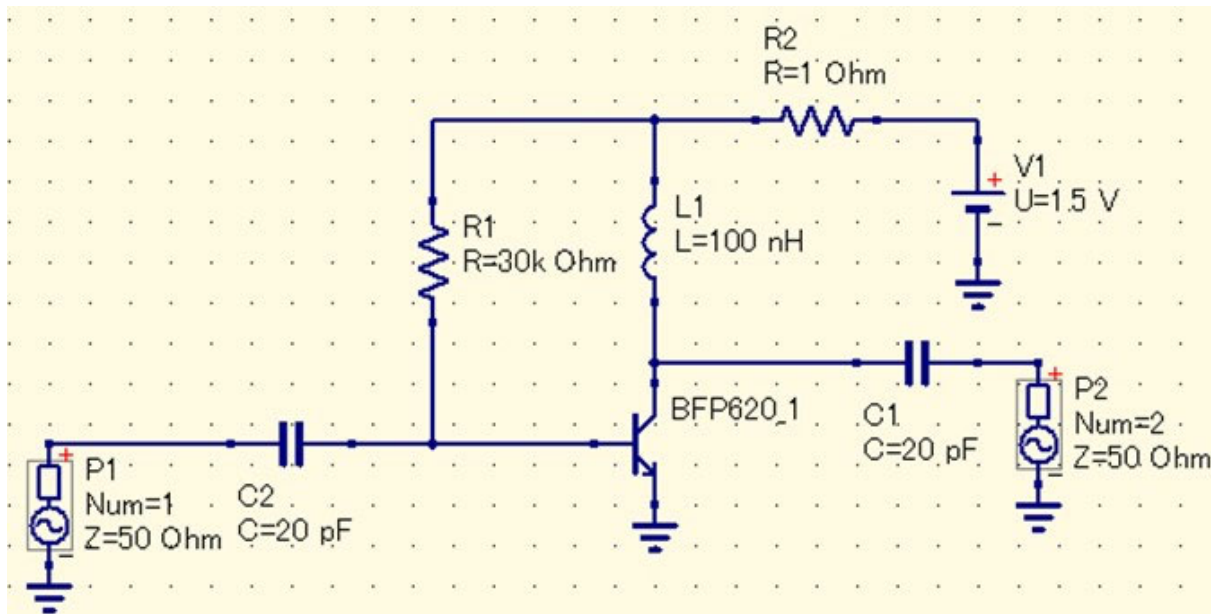
dc simulation

DC1

Equation

Eqn2
Tr=dB(S[2,1])
RL1=dB(S[1,1])
RL2=dB(S[2,2])
NF=log10(F)*10
NFmin=log10(Fmin)*10
K=Rollet(S)

Step 2 S Parameter Simulation



S parameter simulation

SP1
Type=lin
Start=0.5 GHz
Stop=5.5 GHz
Points=2001

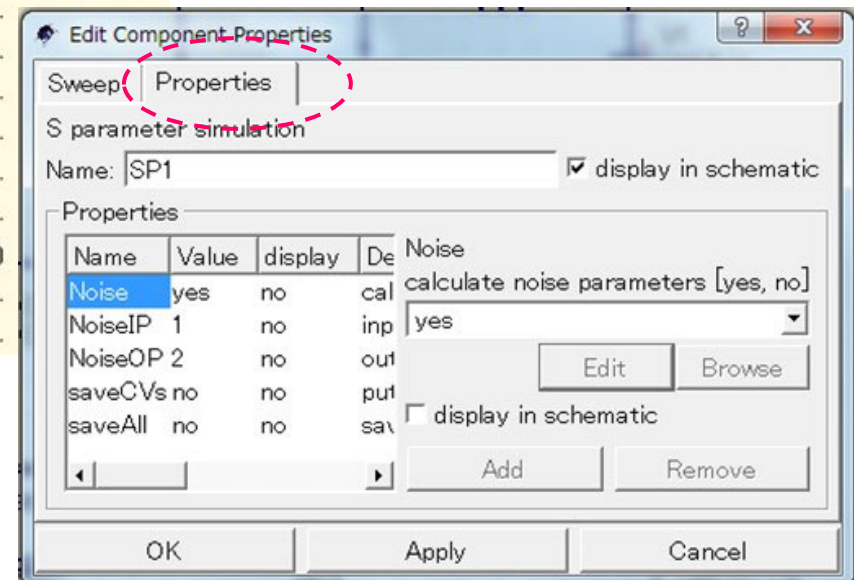
dc simulation

DC1

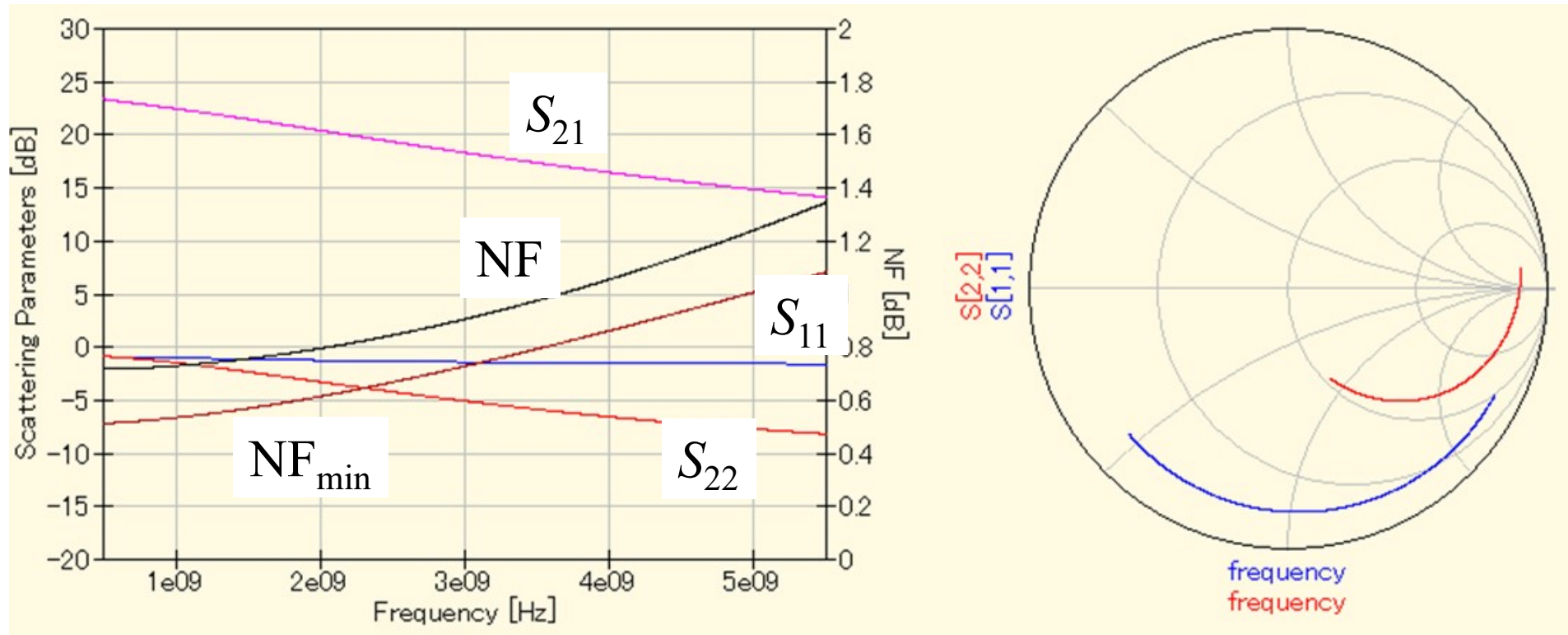
Equation

Eqn2
 $T_r = dB(S[2,1])$
 $RL1 = dB(S[1,1])$
 $RL2 = dB(S[2,2])$
 $NF = \log_{10}(F) * 10$
 $NFmin = \log_{10}(Fmin) * 10$
 $K = Rollet(S)$

Caution!

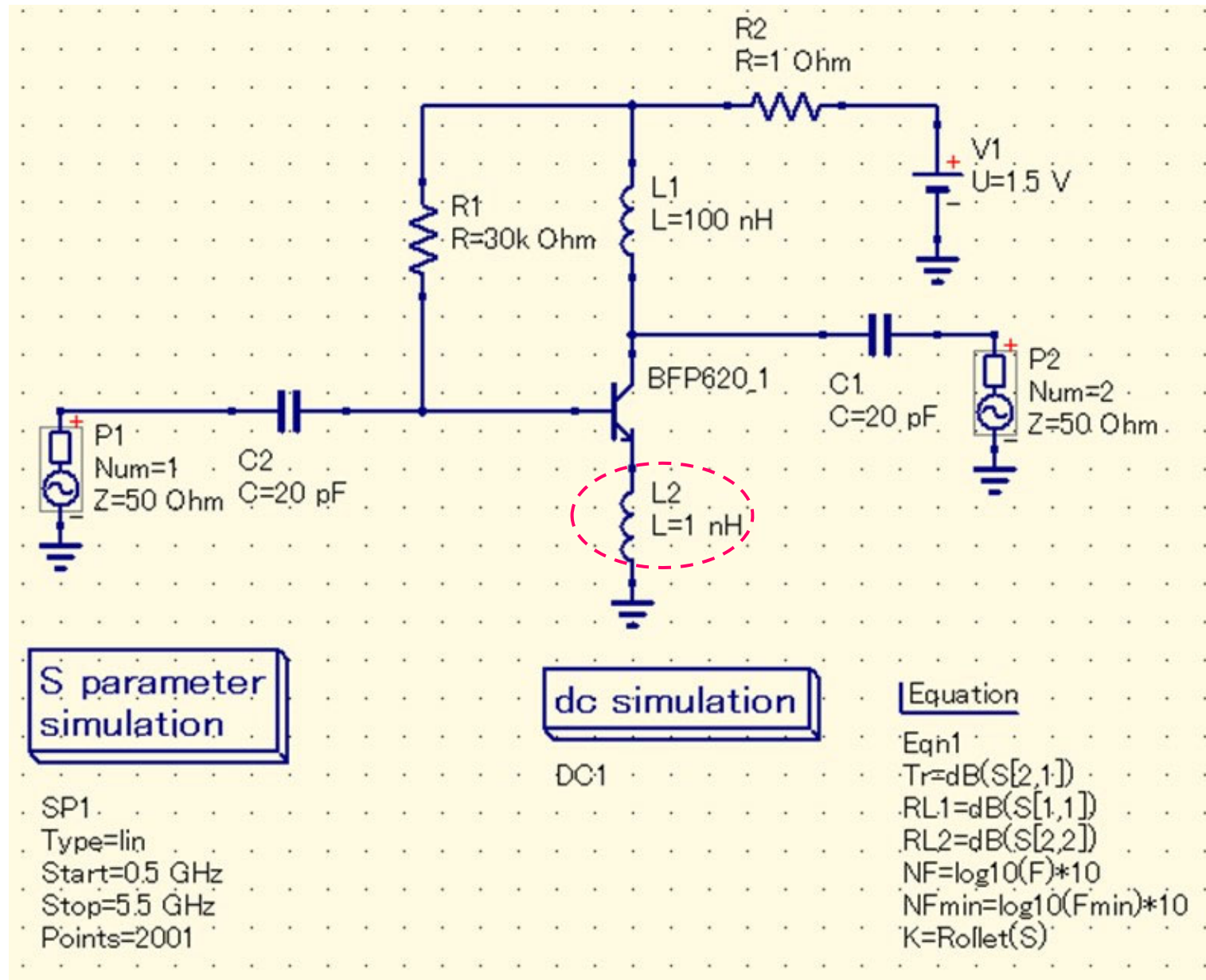


S Simulation Result

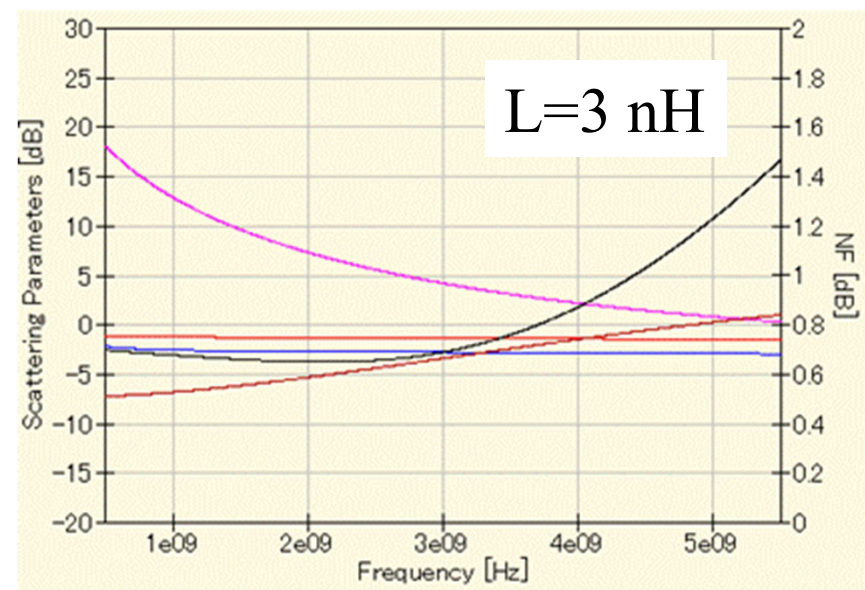
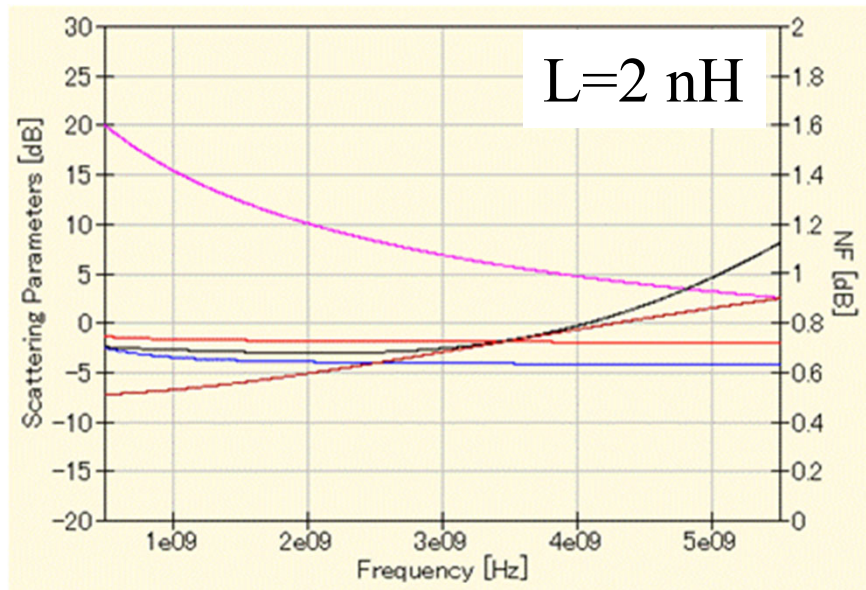
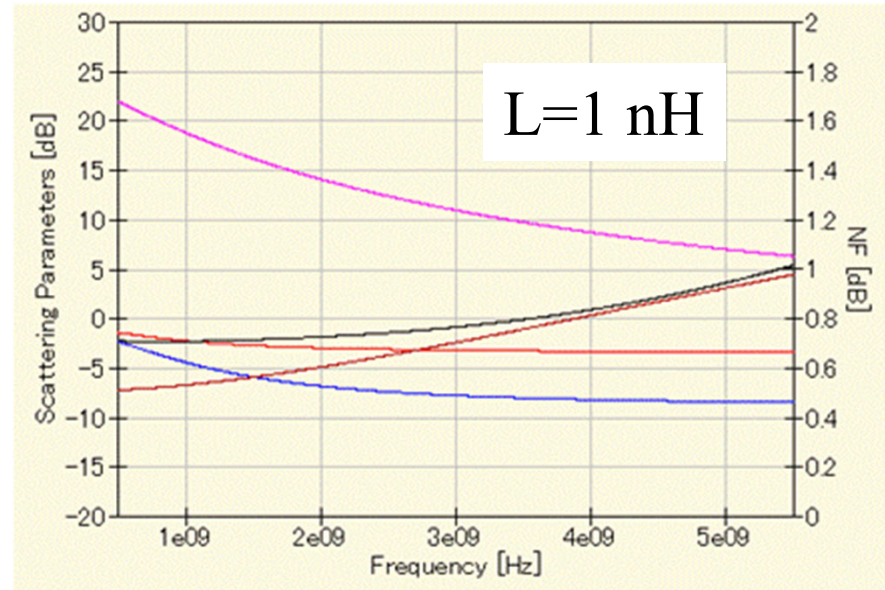
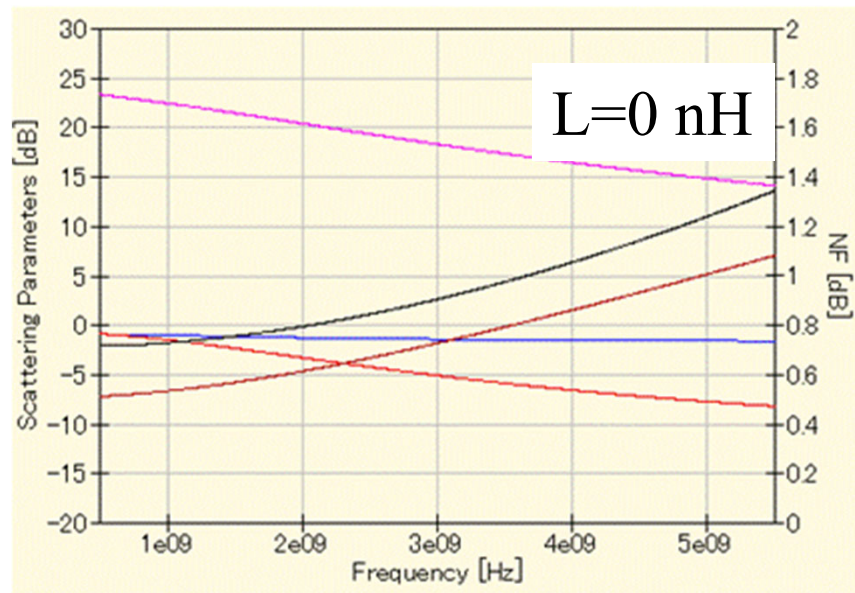


NF_{min}: Achievable minimum NF at the given frequency

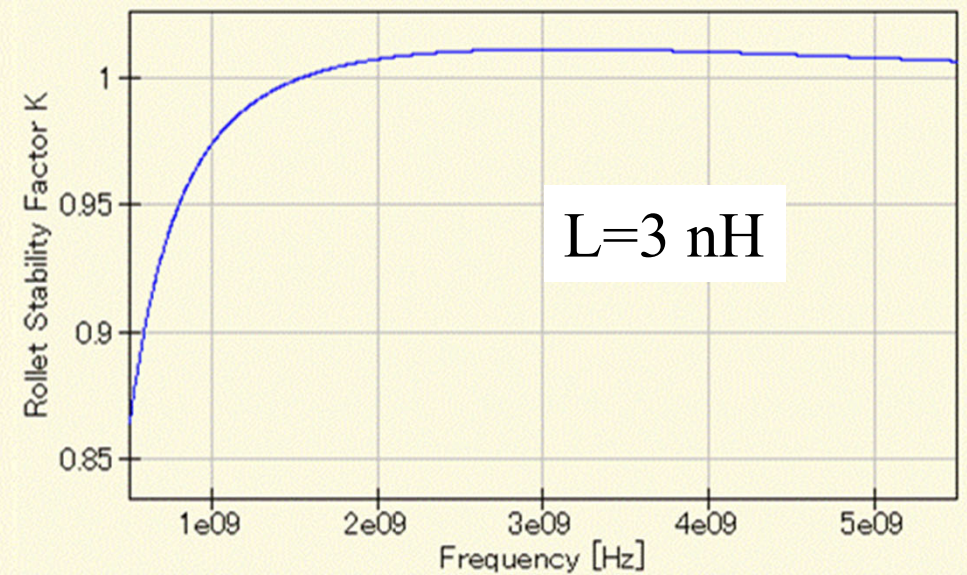
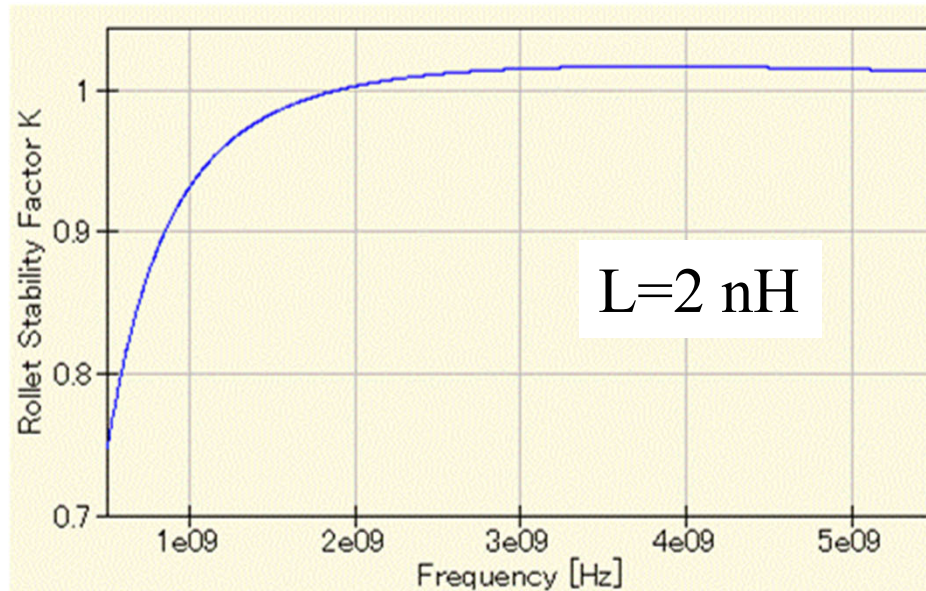
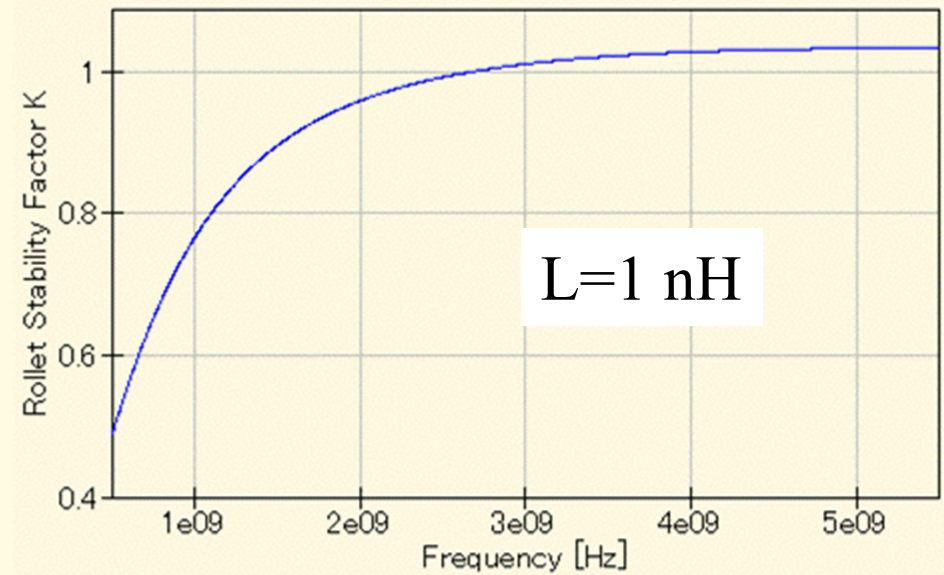
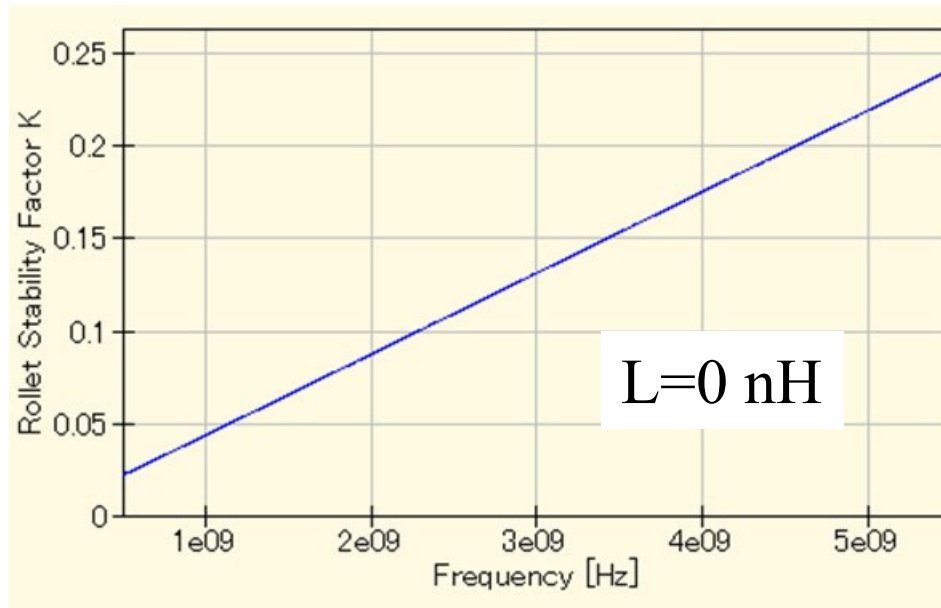
Impact of Emitter Degeneration Inductor



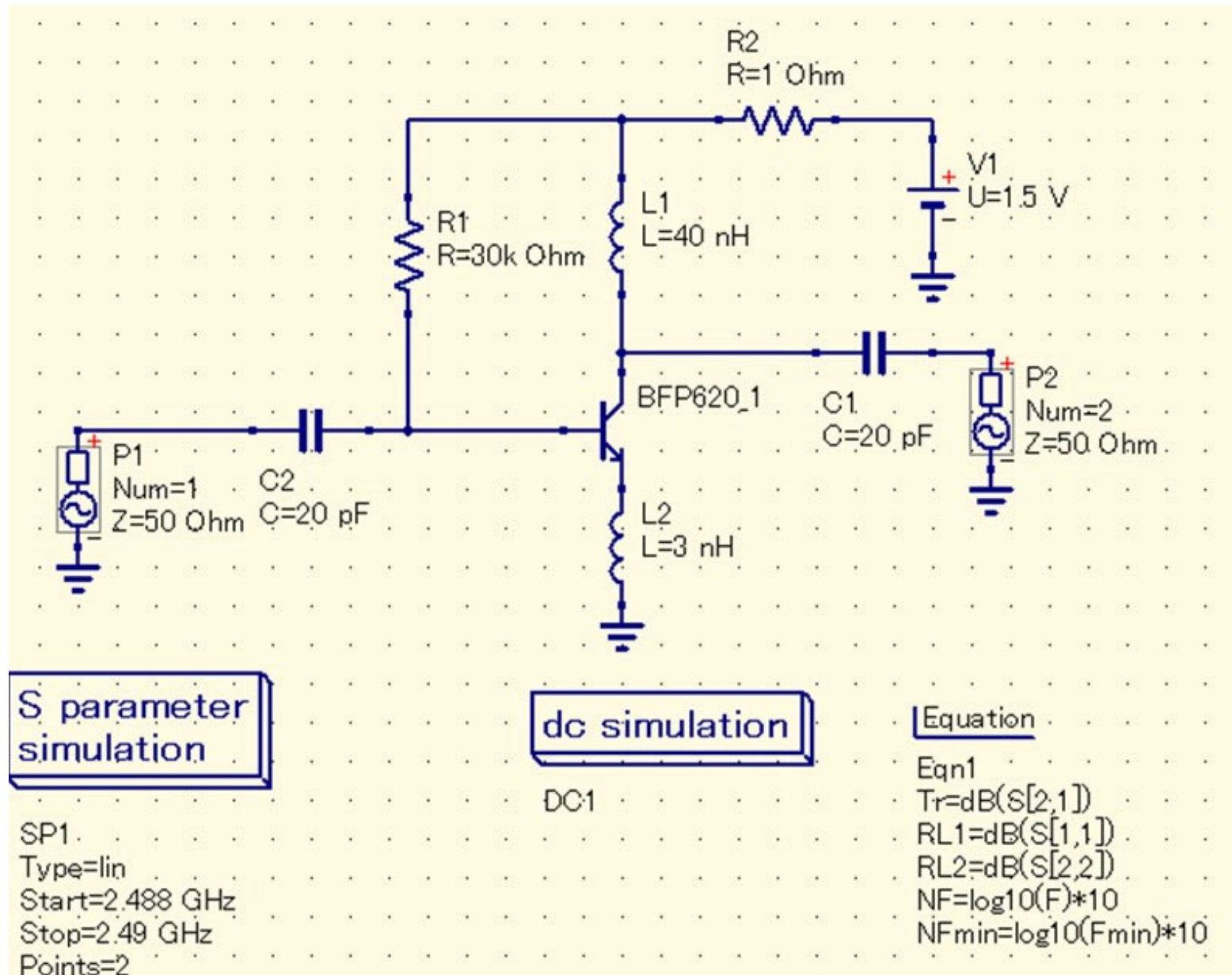
Simulation Results



Simulation Results



Step 3 Design Matching Circuits



Procedure

frequency	S[1,1]	S[1,2]	S[2,1]	S[2,2]
2.49e09	0.732 / -7.84-	0.115 / 87.5-	1.92 / 90.5-	0.861 / 2.03-
2.49e09	0.732 / -7.84-	0.115 / 87.5-	1.92 / 90.5-	0.861 / 2.01-

Create Matching Circuit

☒ calculate two-port matching

Reference Impedance

Port 1 ohms Port 2 ohms

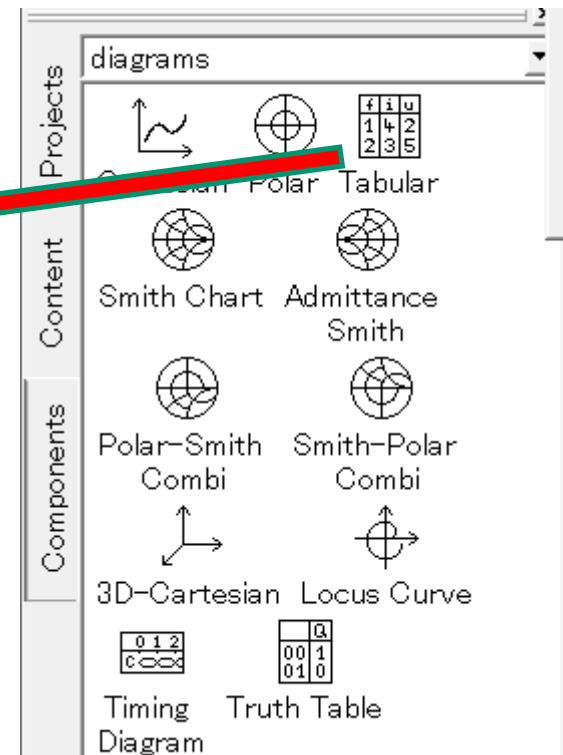
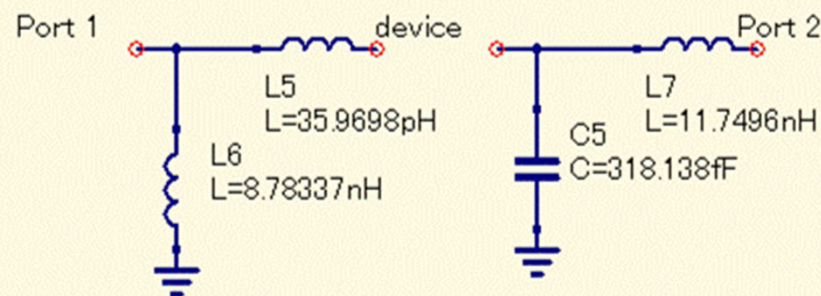
S Parameter

Input format

S11 / - S12 / -

S21 / - S22 / -

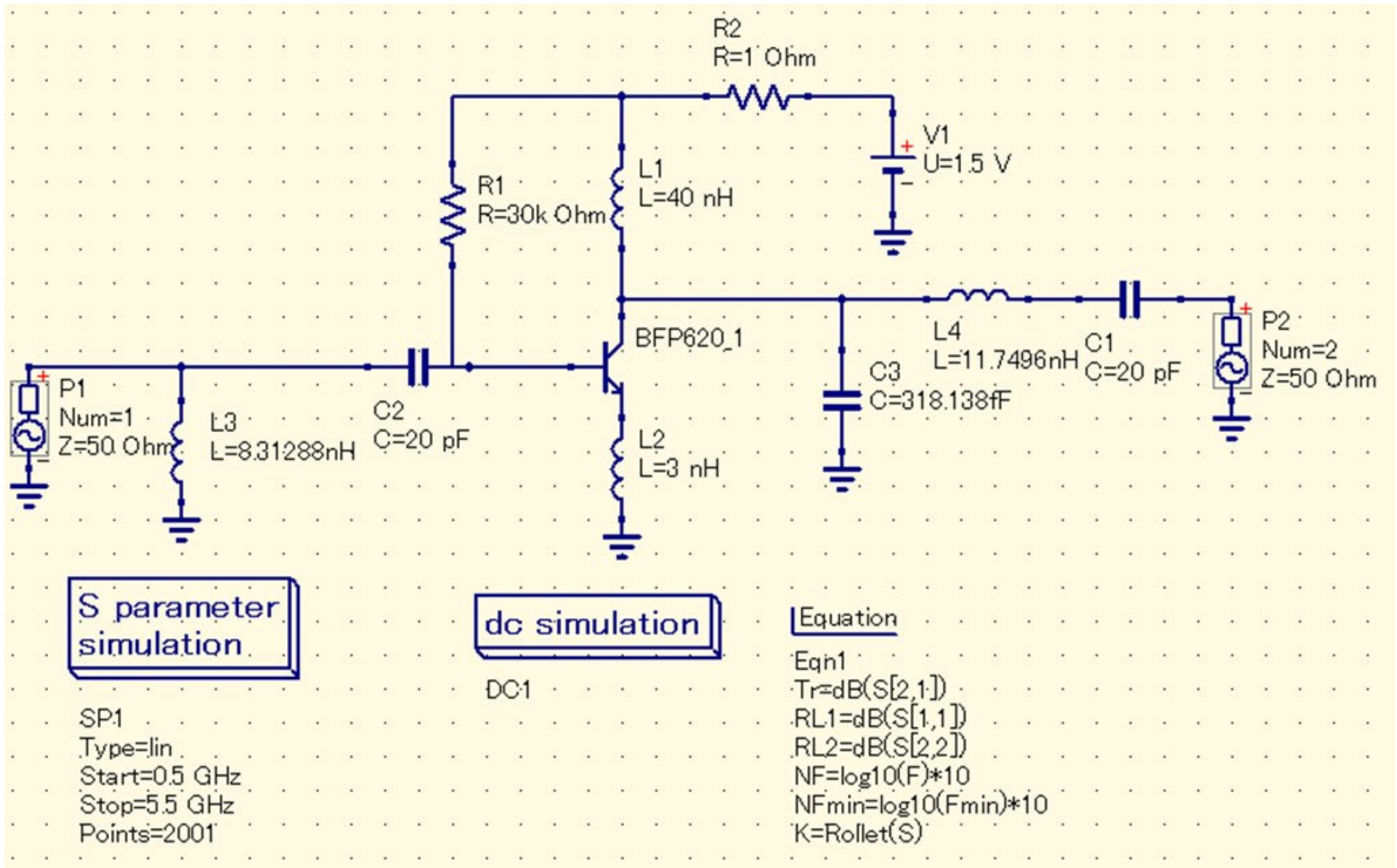
Frequency: GHz



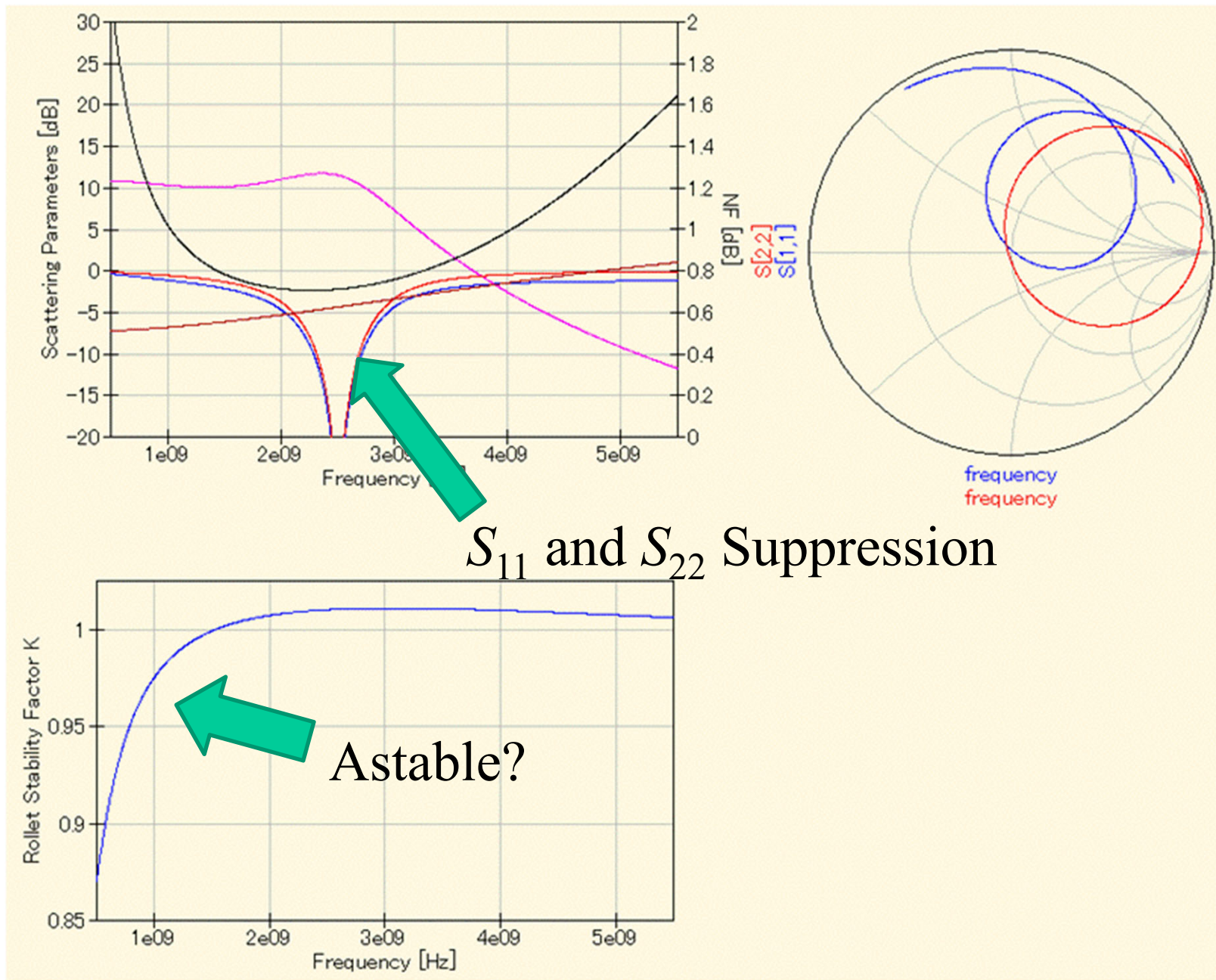
RF Circuit Basics_SJTU - Po

Tools	Simulation	View	Help
Text Editor			Ctrl+1
Filter synthesis			Ctrl+2
Line calculation			Ctrl+3
Component Library			Ctrl+4
<u>Matching Circuit</u>			Ctrl+5
Attenuator synthesis			Ctrl+6

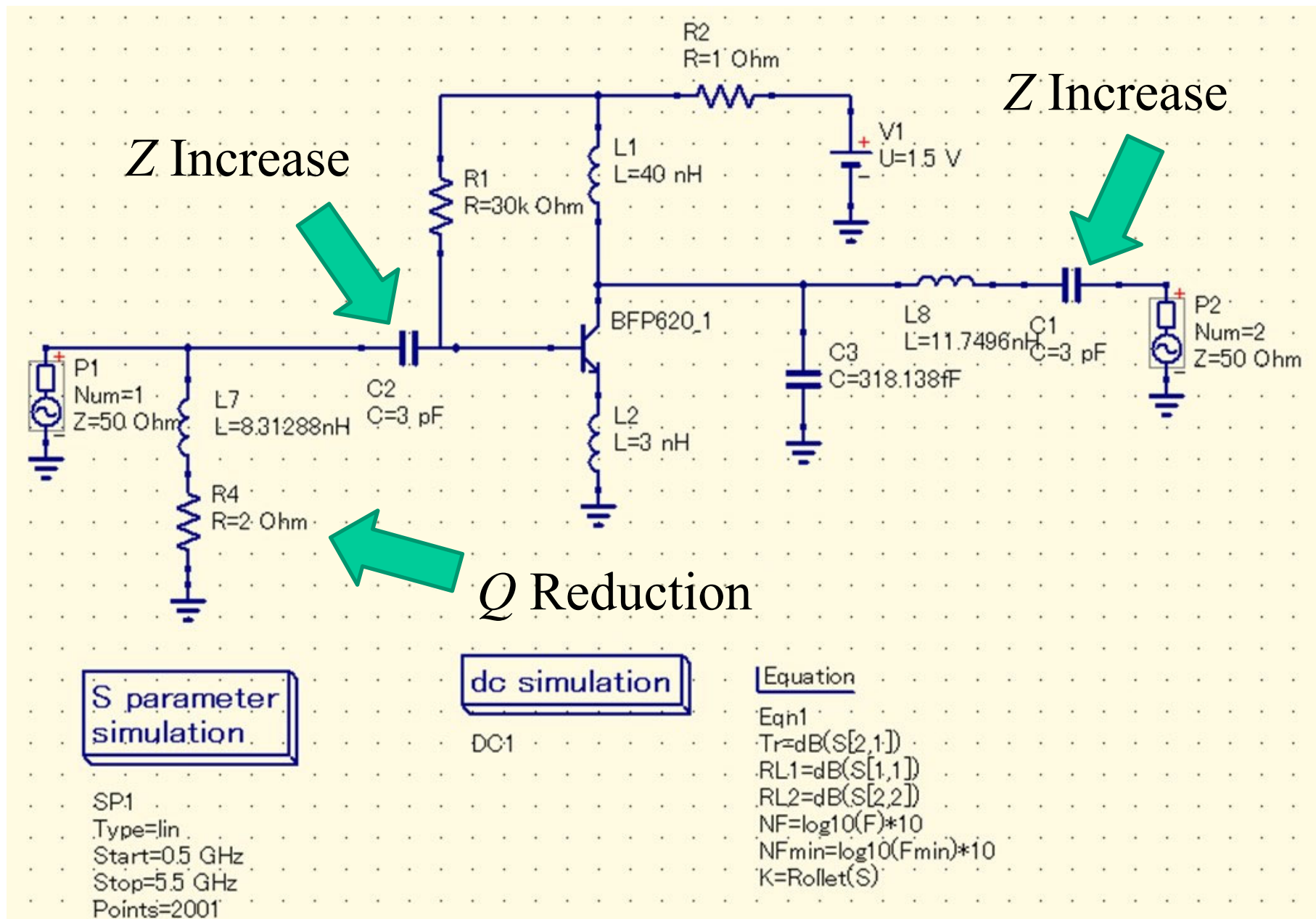
After Adding Designed Matching Circuit



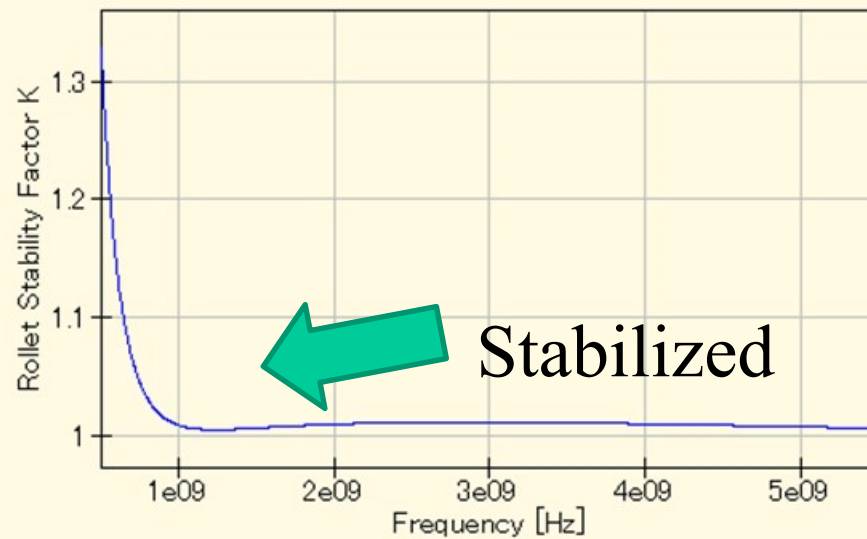
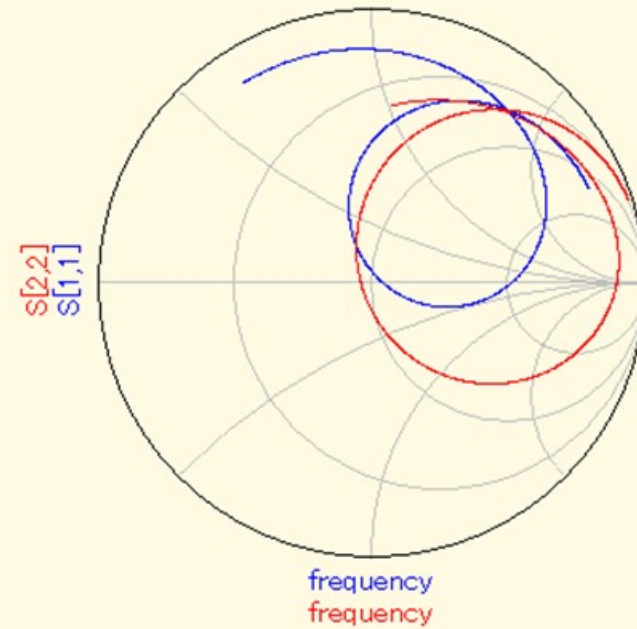
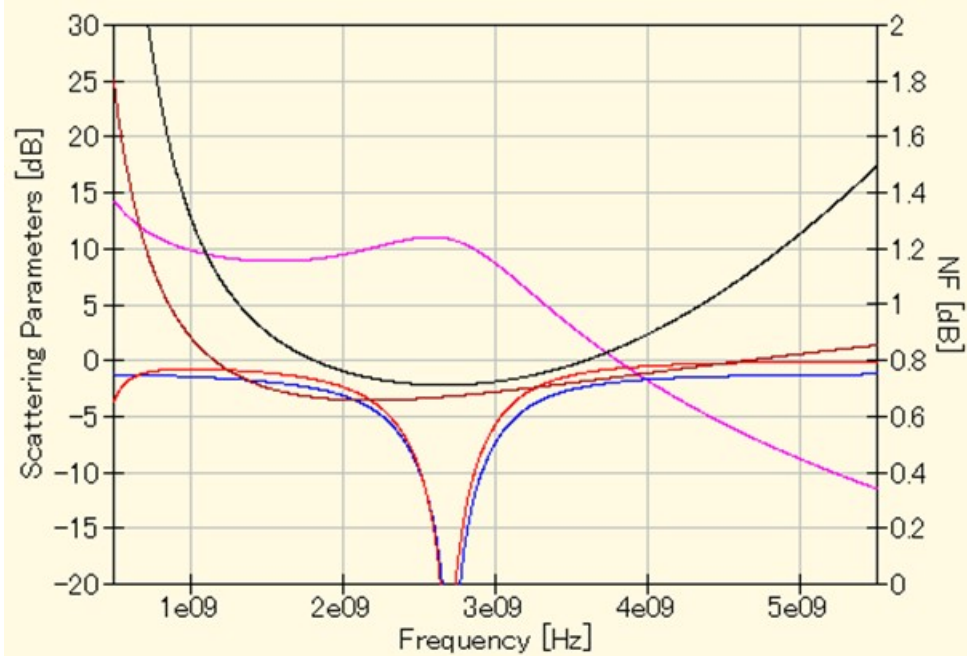
Simulated Results



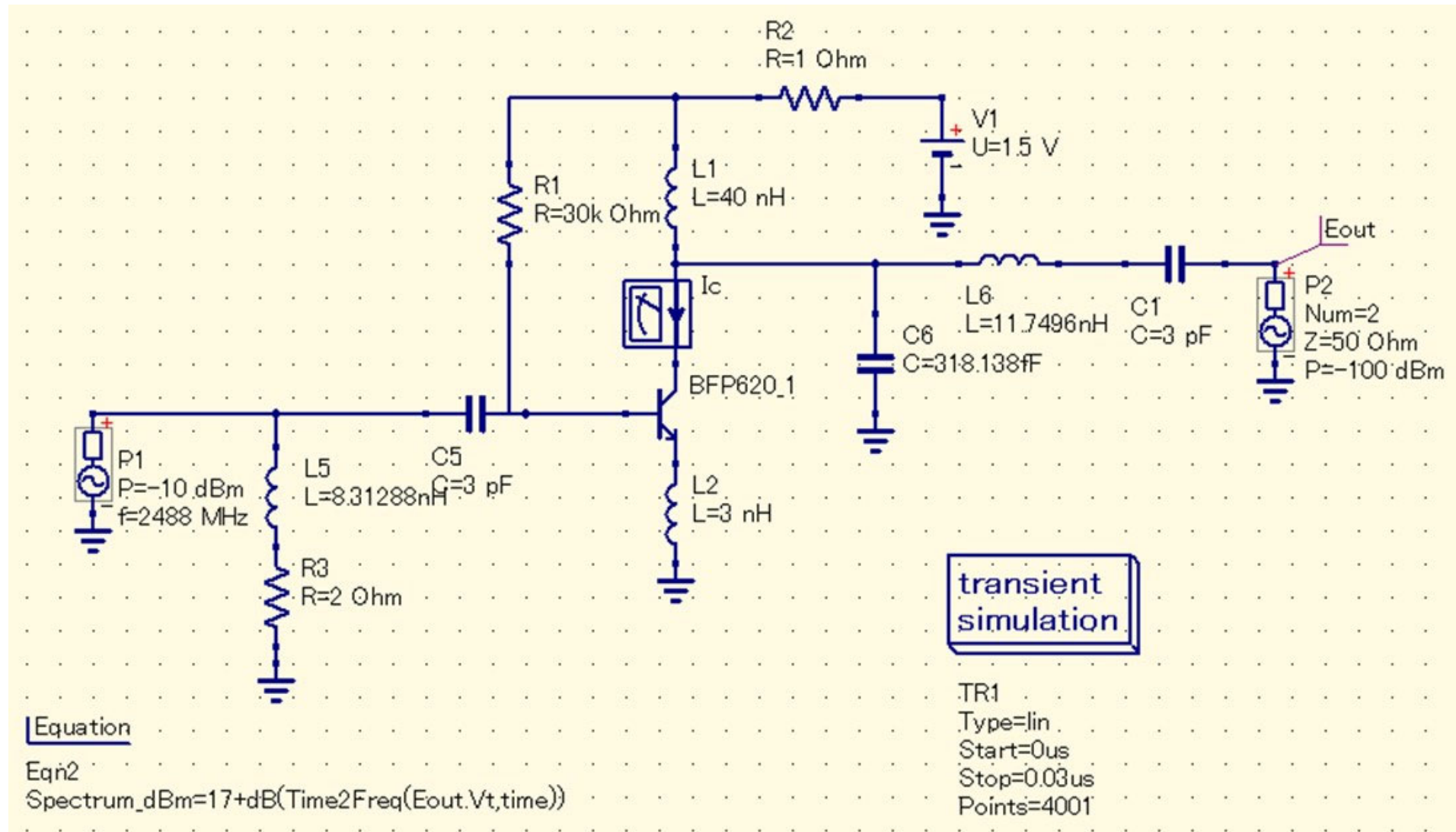
Step 4 Stabilization



Simulation Results

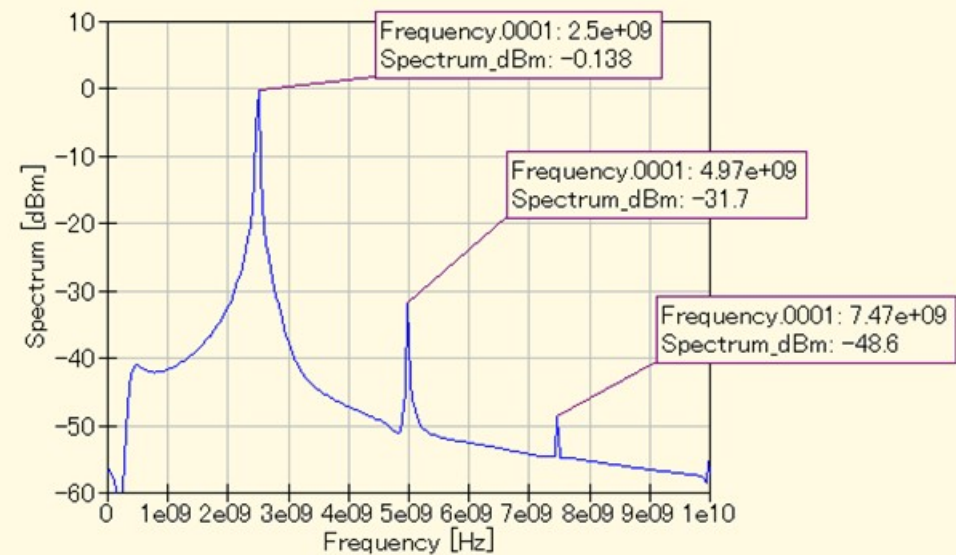
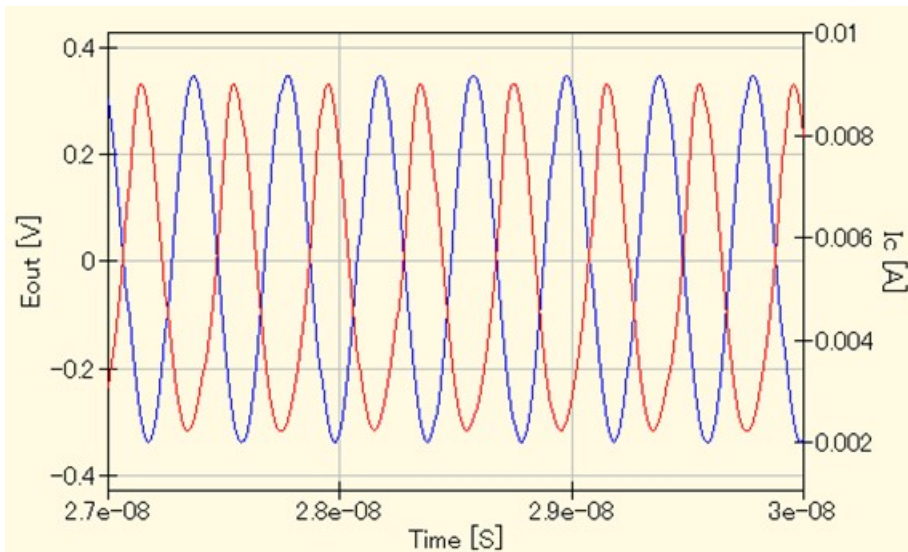


Step 5 Transient Analysis

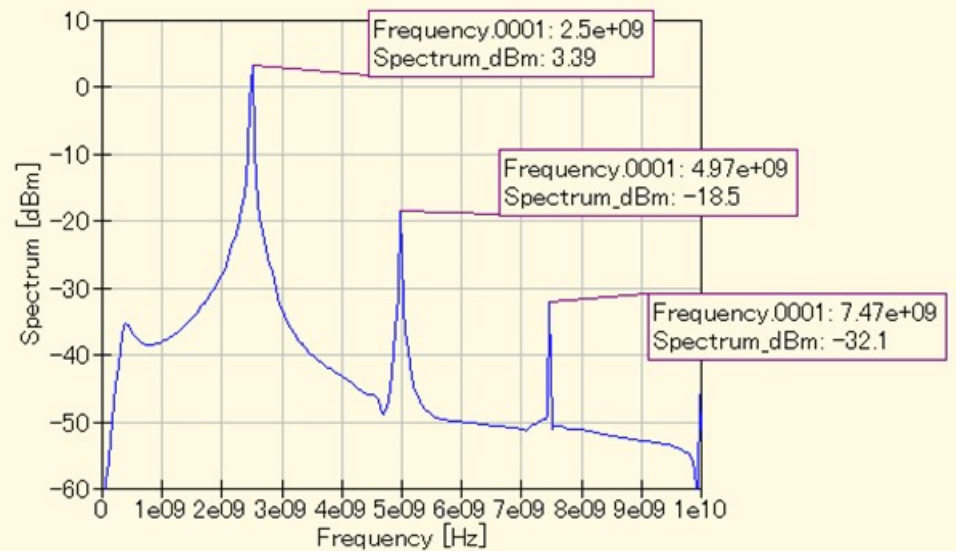
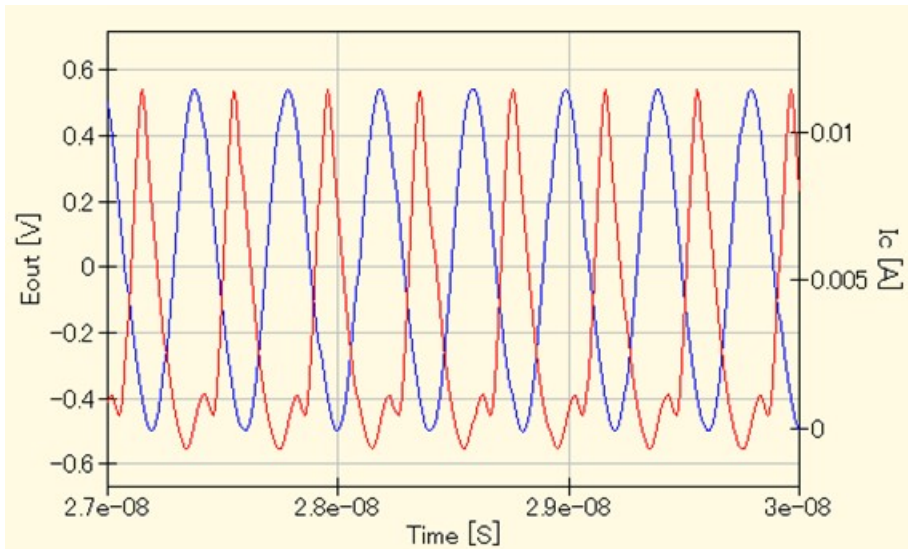


Simulation Results

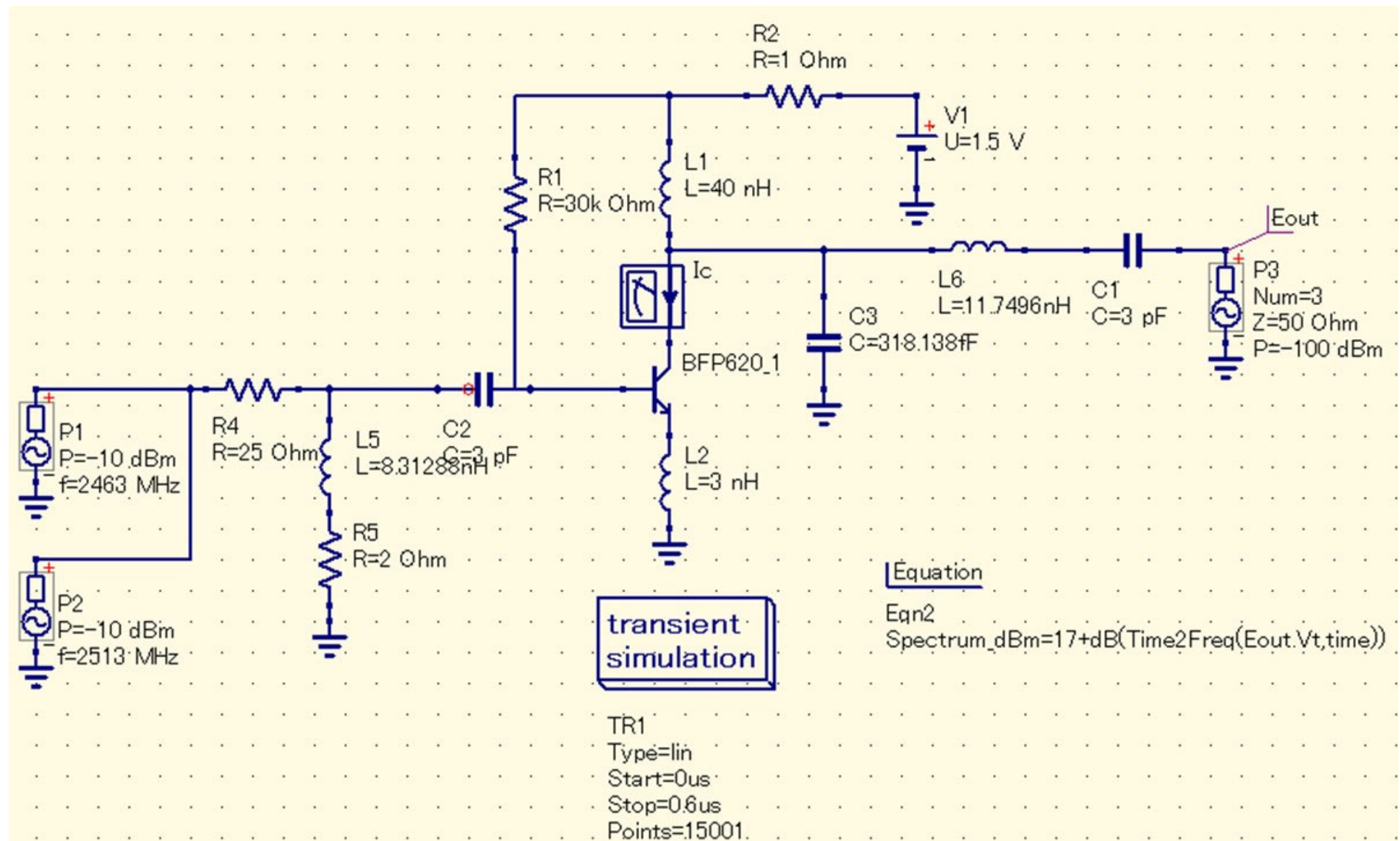
$P_{in} = -10$ dBm



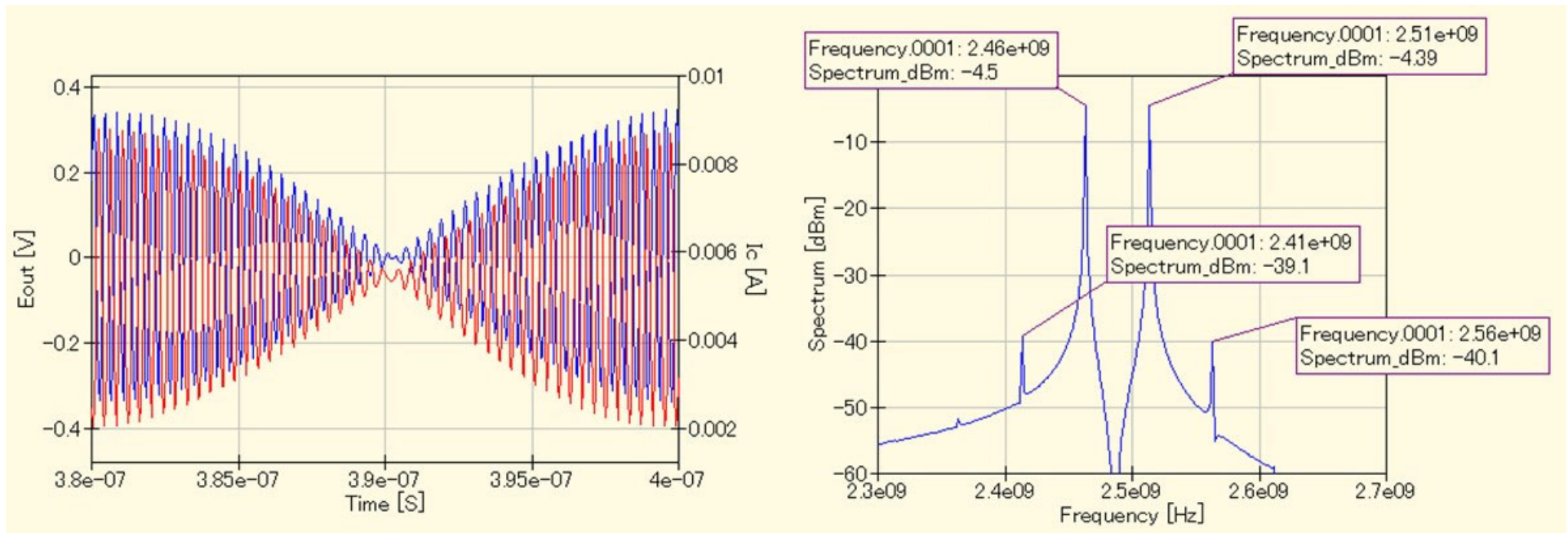
$P_{in} = -5$ dBm



Step 6 Two Tone Analysis



Two Tone Test Result



$$P_{2a\pm b} [\text{dBm}] = 2 \times P_a [\text{dBm}] + P_b [\text{dBm}] - 2 \times \text{OIP3} [\text{dBm}]$$

➡ $-40.1 = 2 \times (-4.39) + (-4.5) - 2 \times \text{OIP3}$

➡ $\text{OIP3} = 13.4 [\text{dBm}]$